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## AAP11/AAP21

### Schematic Document

SKL-H paltform with Nvidia N16E-GS/GT/GX

Rev: 1.0(A00) PVT

2015/07/21

@ : Nopop Component

EMI@ /@EMI@ : EMI pop/unpop part  
ESD@ /@ESD@ : ESD pop/unpop part  
RF@ /@RF@ : RF pop/unpop part

CONN@ : Connector Component

AOAC@ : Intel AOAC  
DS3/NODS3: deepS3  
TBT@: ThunderBolt  
PD@: Power Delivery

DIS@ : Discrete Part

N16EGS@:N16E-GS(2G)  
N16EGT@:N16E-GT(3G)  
N16EGX@:N16E-GX(4G)  
2G@:2G VRAM  
3G@:3G VRAM  
4G@:4G VRAM

DAX PCB  
DAZ18F00100  
PCB 18F LA-B752P REV0 M/B 8  
R1@

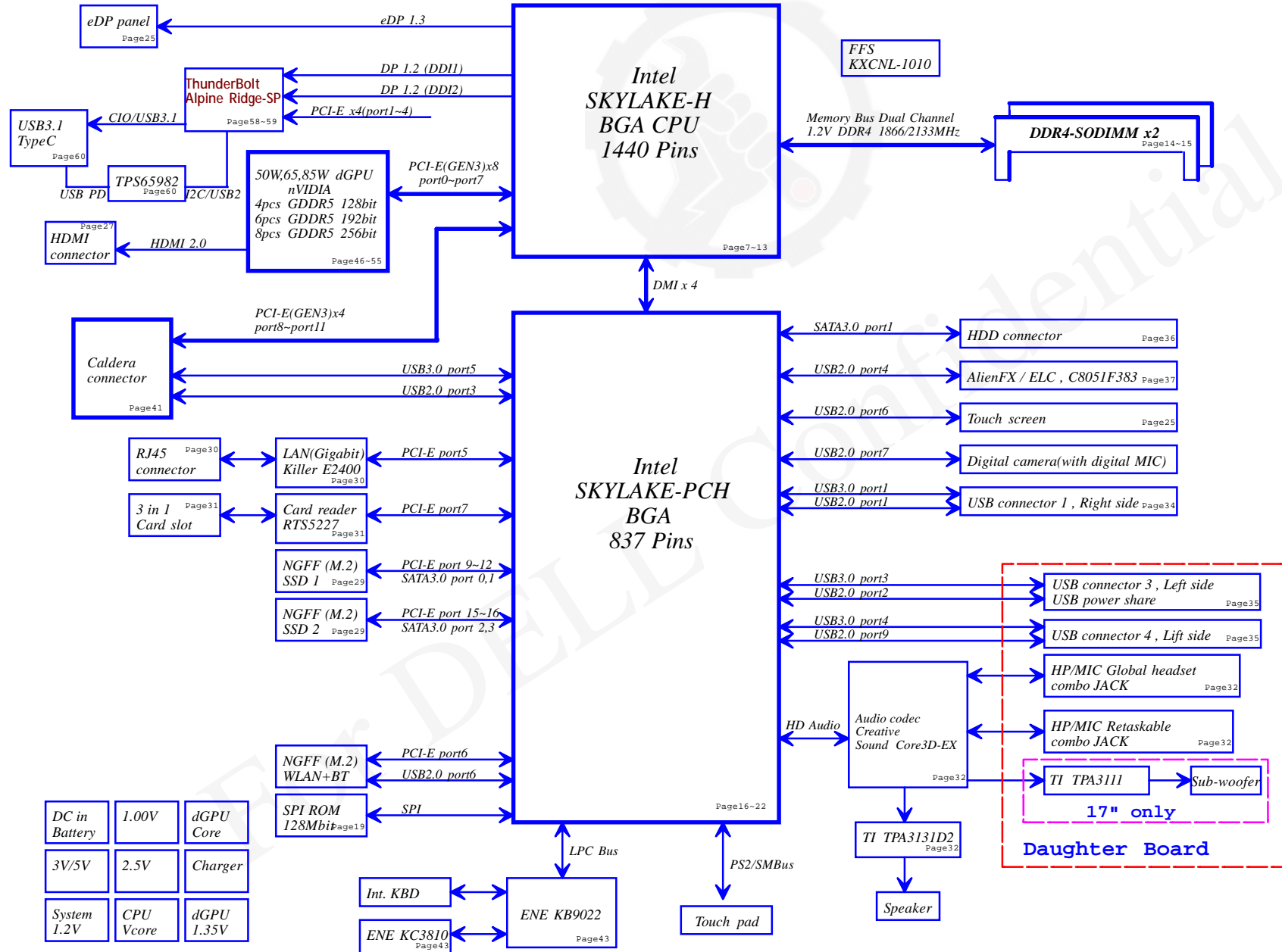
DAX PCB  
DAZ18F00101  
PCB 18F LA-B752P REV0 M/B 8  
R3@

12L

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				Custom	LA-C912P
				Date:	Wednesday, July 22, 2015
				Sheet	1 of 78
				Rev	0.1

# SKL+NV Block Diagram

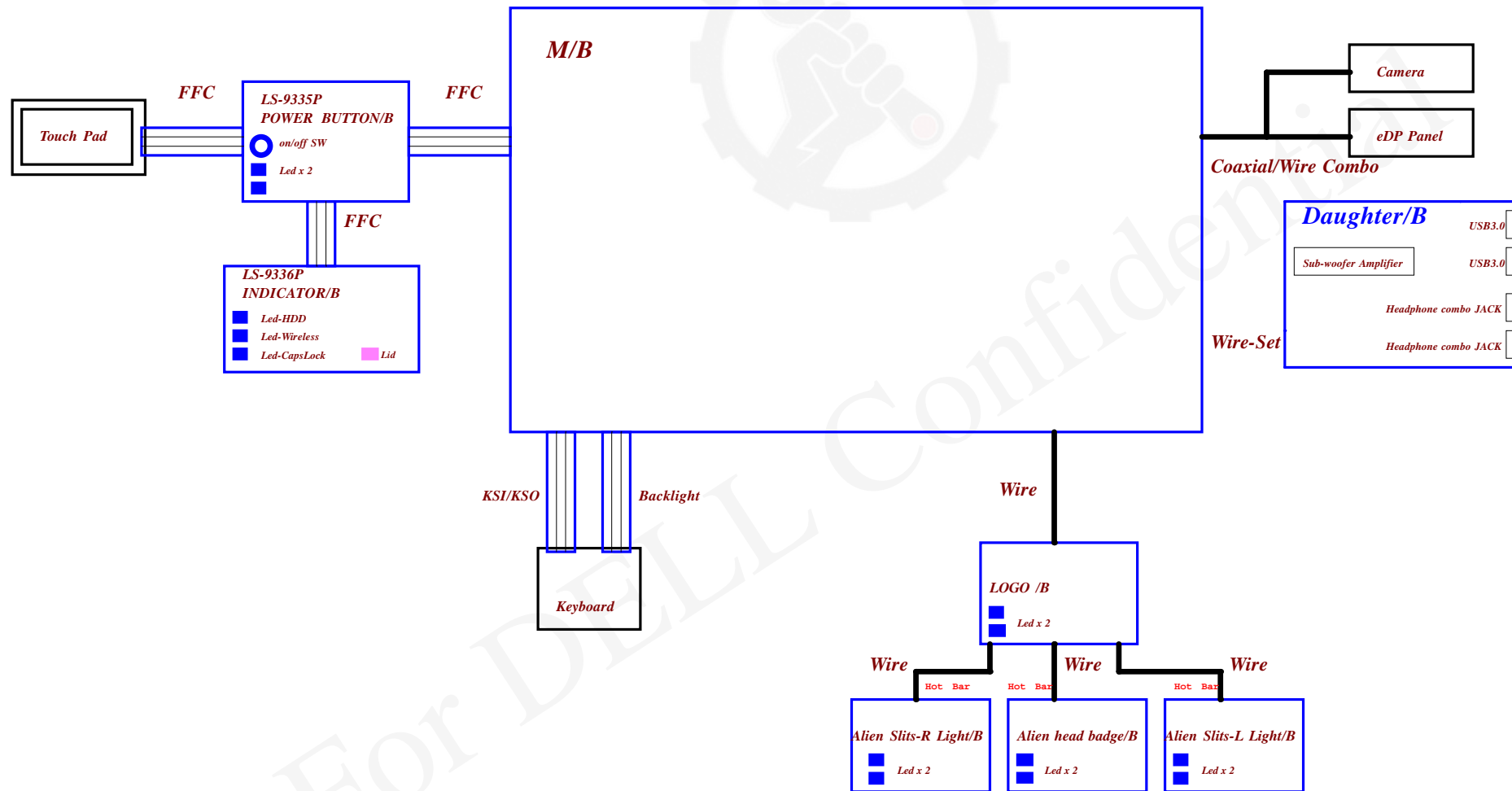
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				Rev	0.1
				Sheet	2 of 78

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Size		Document Number		Rev	
Date: Wednesday, July 22, 2015		Sheet 3 of 78		0.1	

Board ID Table for AD channel

Vcc	3.3V +/- 1%					
Ra	100K +/- 1%					
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3	
0	0	0.000V	0.000V	0.300V	0x00 - 0x0B	
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C	
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26	
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30	
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B	
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46	
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54	
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64	
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76	
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87	
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96	
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3	
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD	
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7	
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0	
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9	
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3	
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC	
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6	
19	NC	3.000V	3.300V	3.300V	0xE7 - 0xFF	

Board ID TABLE

ID	PCB Revision
NV	AMD
0	10
1	11
2	12
3	13
4	14
5	15

TBT connector change to SMD type.

Symbol Note :

 : means Digital Ground

 : means Analog Ground

CLOCK SIGNAL	
CLKOUT_PCIE0	
CLKOUT_PCIE1	
CLKOUT_PCIE2	10/100/1000 LAN
CLKOUT_PCIE3	M.2 Card WLAN
CLKOUT_PCIE4	dGPU (N16)
CLKOUT_PCIE5	DGPU (Caldera)

USB3.0

Port1	Right side1
Port2	Right side2
Port3	Left side 1
Port4	
Port5	Caldera
Port6	Left side 2

USB2.0

Port0	Right side1
Port1	Left side 1 (PowerShare)
Port2	Caldera
Port3	ELC
Port4	BT
Port5	Touch screen
Port6	Camera
Port7 / 8	Right side 2 Left side 2

PCI EXPRESS

Lane 1	
Lane 2	
Lane 3	10/100/1000 LAN
Lane 4	M.2 Card WLAN
Lane 5	PCIE 4x MUX
Lane 6	

SATA

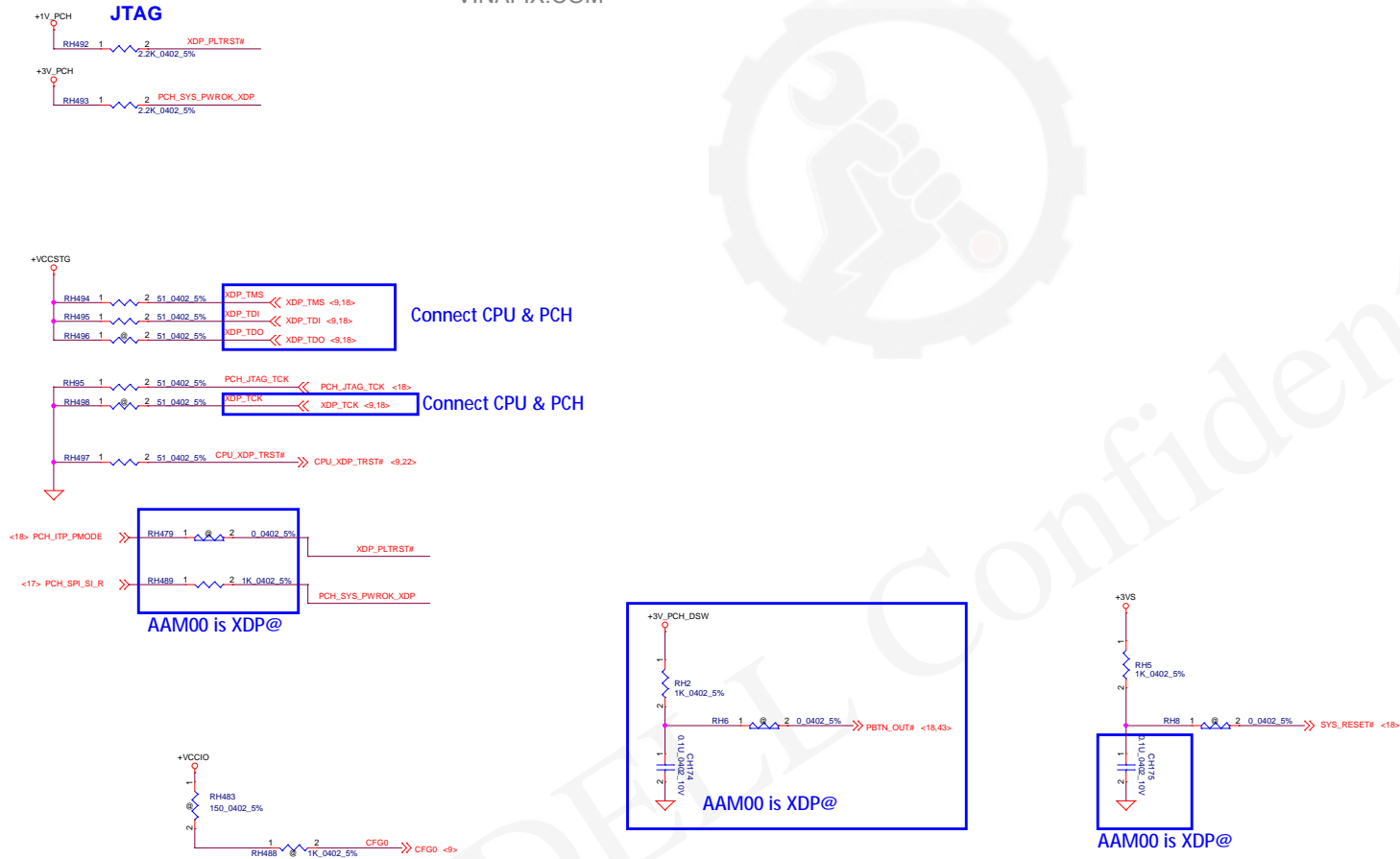
SATA0	HDD
SATA1	NGFF SSD
SATA2	NGFF SSD
SATA3	

BDW

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				Date	Wednesday, July 22, 2015
				Sheet	4 of 78
				Rev	0.1



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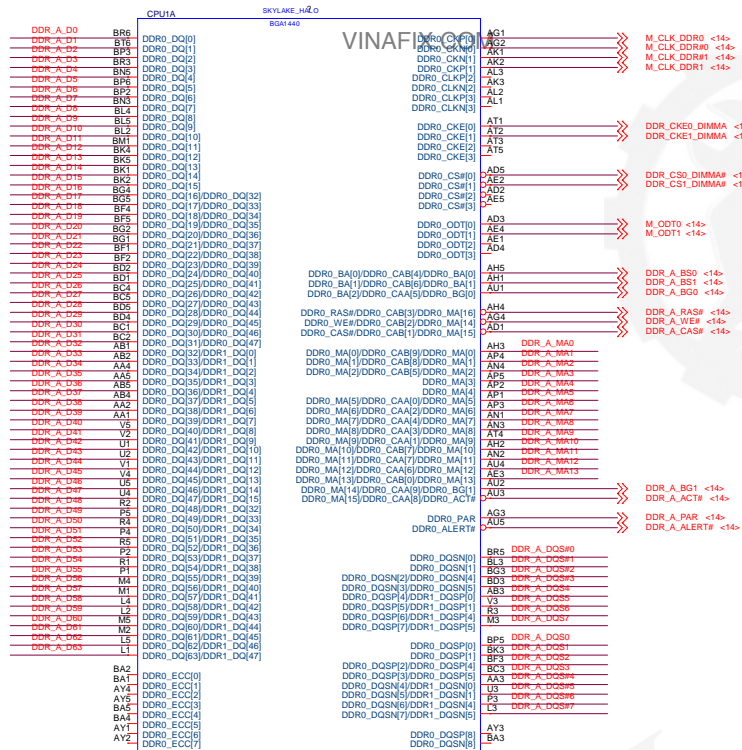
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Size		Document Number		Rev	
Date: Wednesday, July 22, 2015		Sheet 6 of 78		0.1	



## Interleave

<14> DDR\_A.DQ[0..63]  
<14> DDR\_A.MA[0..13]  
<14> DDR\_A.DQS[0..7]  
<14> DDR\_A.DQS[0..7]

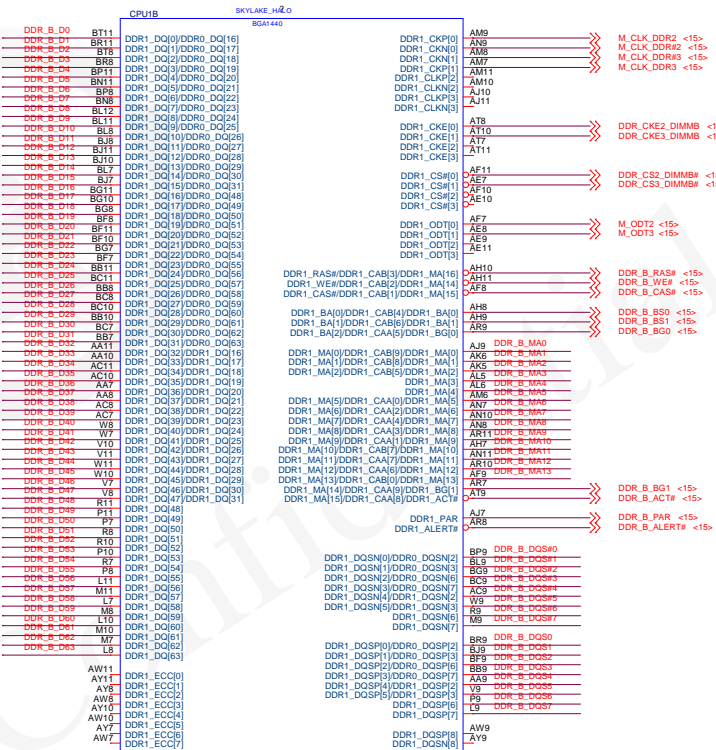
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<15> DDR\_B.MA[0..13]  
<15> DDR\_B.DQS[0..7]  
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DDR CHANNEL A

SKL-H.BGA1440 REV=1

1-OF-14



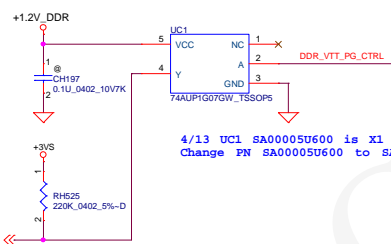
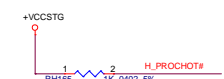
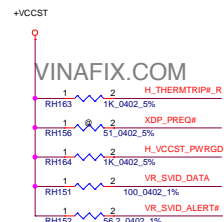
DDR CHANNEL B

SKL-H.BGA1440 REV=1

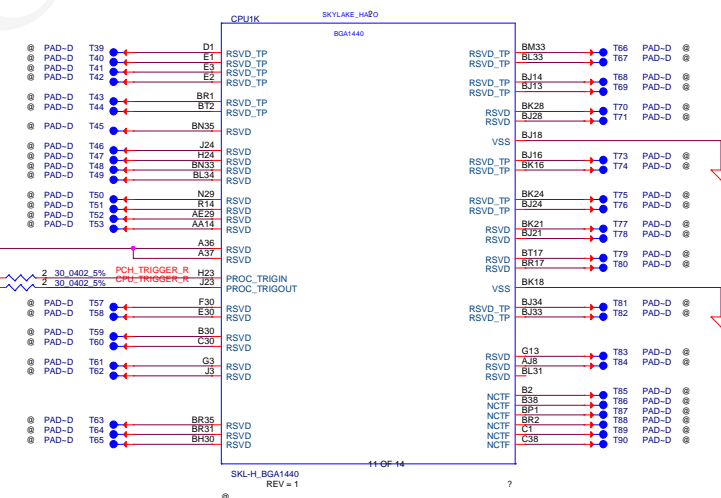
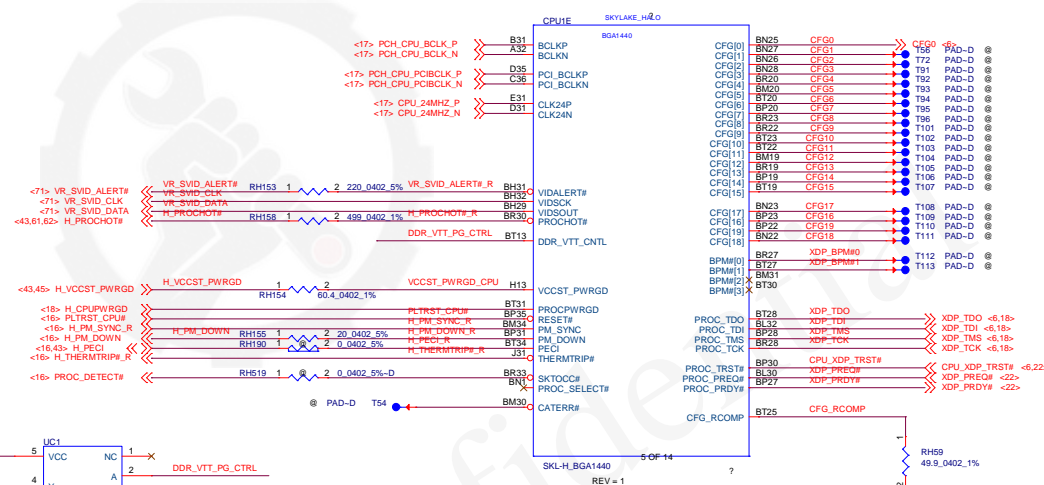
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				Sheet	8 of 78
				Rev	0.1

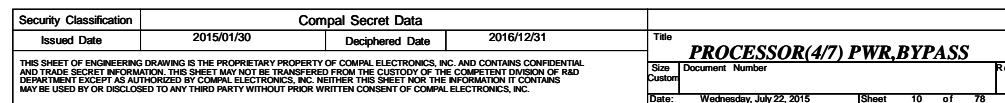


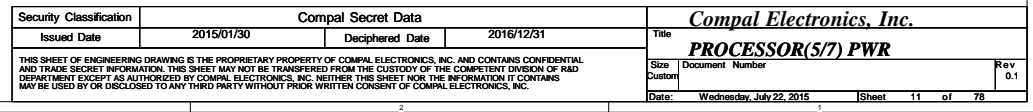


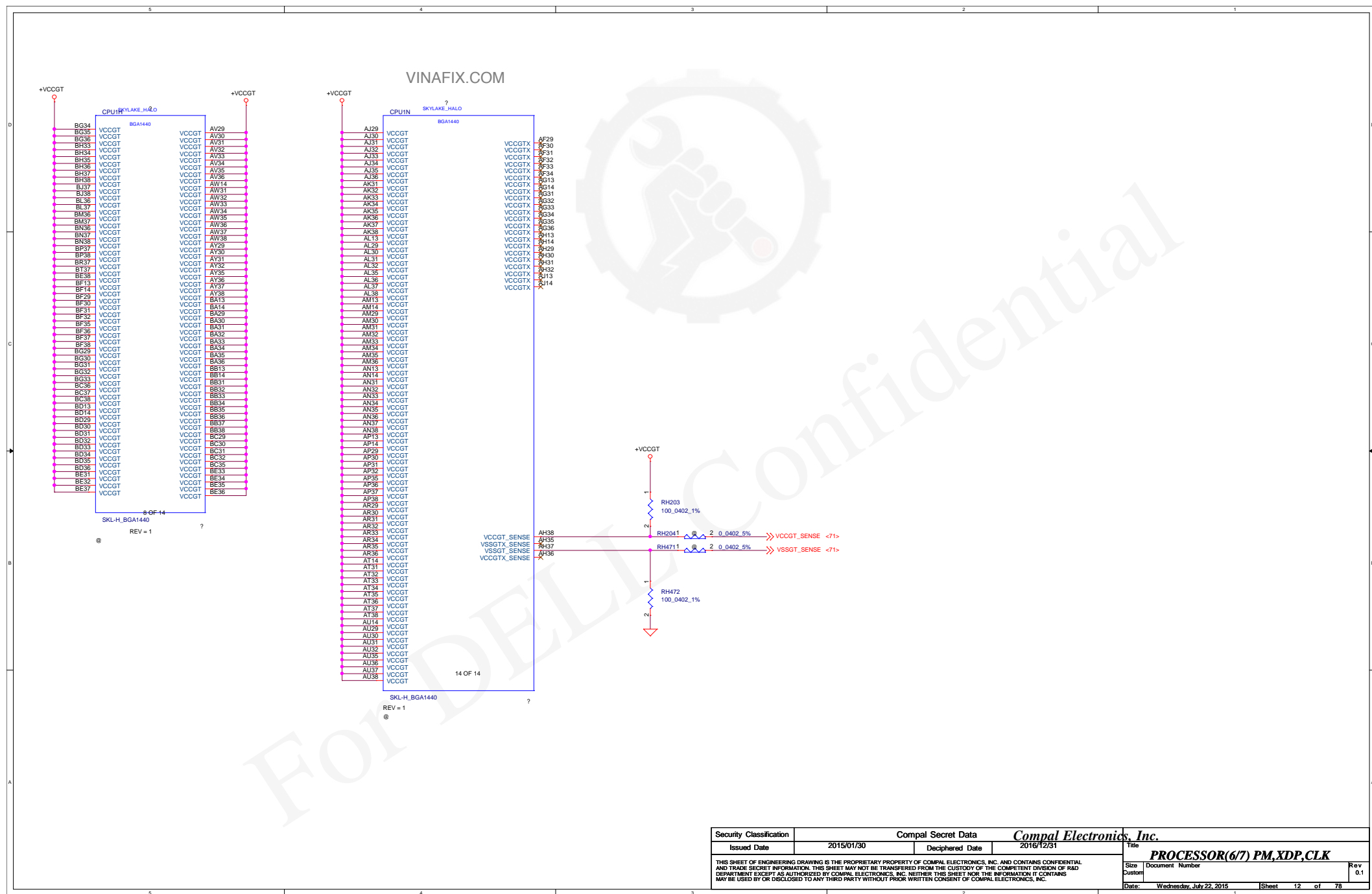
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Change PN SA00005U600 to SA00007WE00.

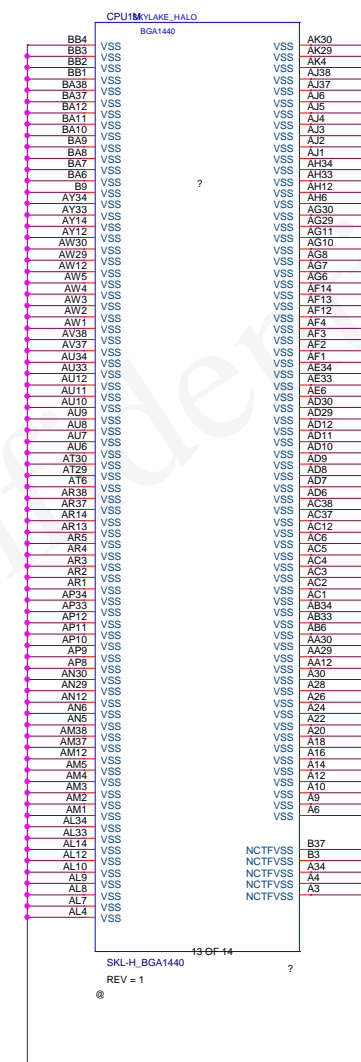
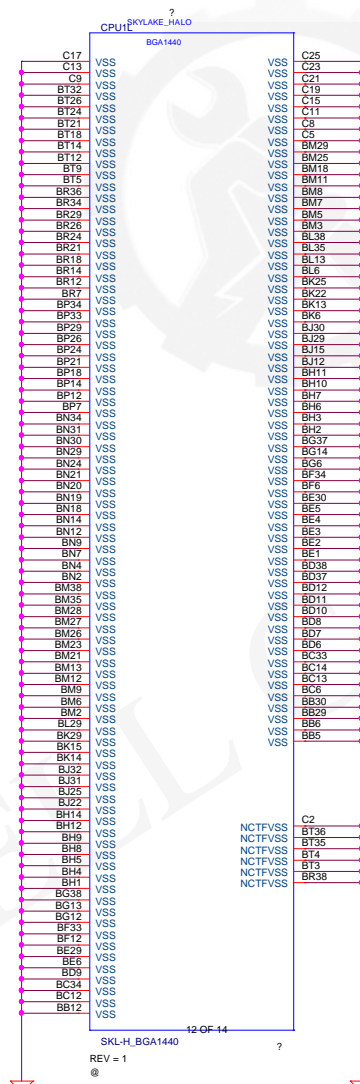


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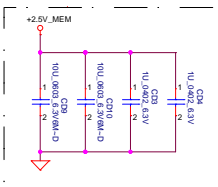




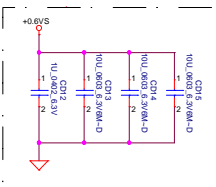


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Layout Note:  
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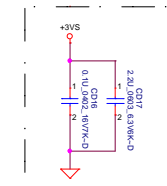


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Place near JDIMM1.258

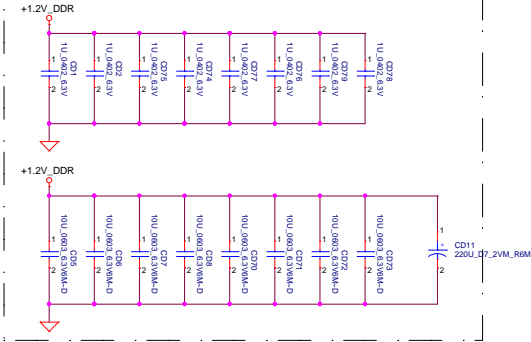


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Layout Note:  
Place near JDIMM1.255



Layout Note:  
Place near JDIMM1



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<> DDR\_A\_BG1

<> DDR\_A\_BG0

<> M\_CLK\_DDR0

<> M\_CLK\_DDR0#

<> DDR\_A\_PAR

<> DDR\_A\_PAR#

<> DDR\_CS0\_DIMM#

<> DDR\_A\_WE#

<> M\_ODT0

<> DDR\_CS1\_DIMM#

<> M\_ODT1

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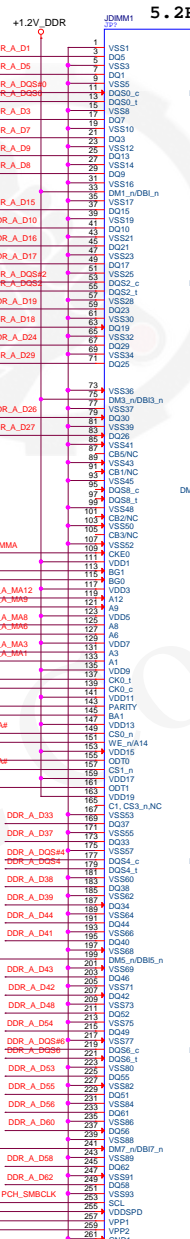
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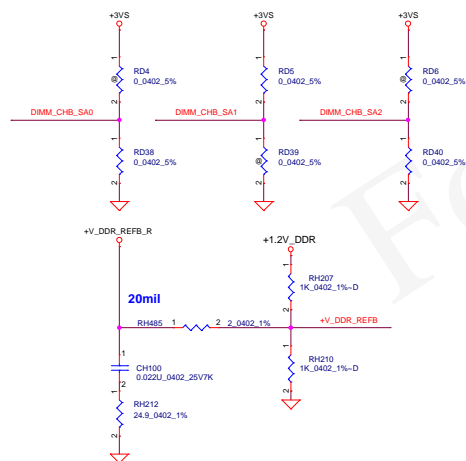
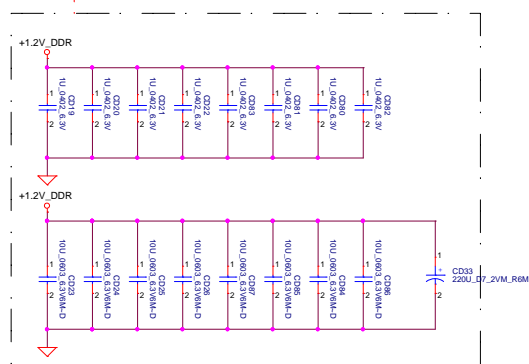
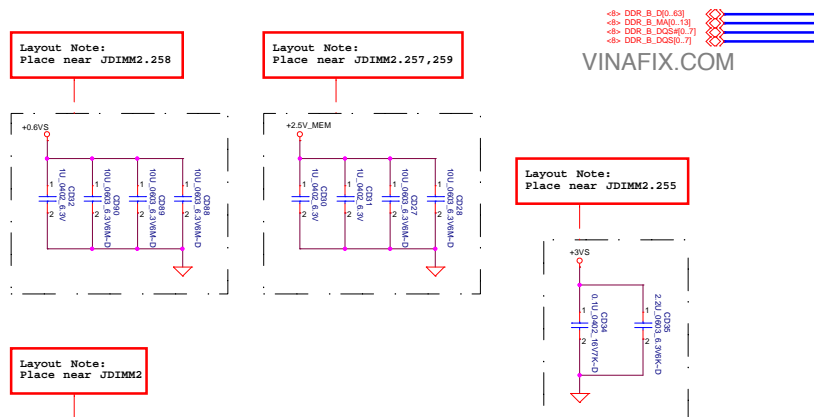
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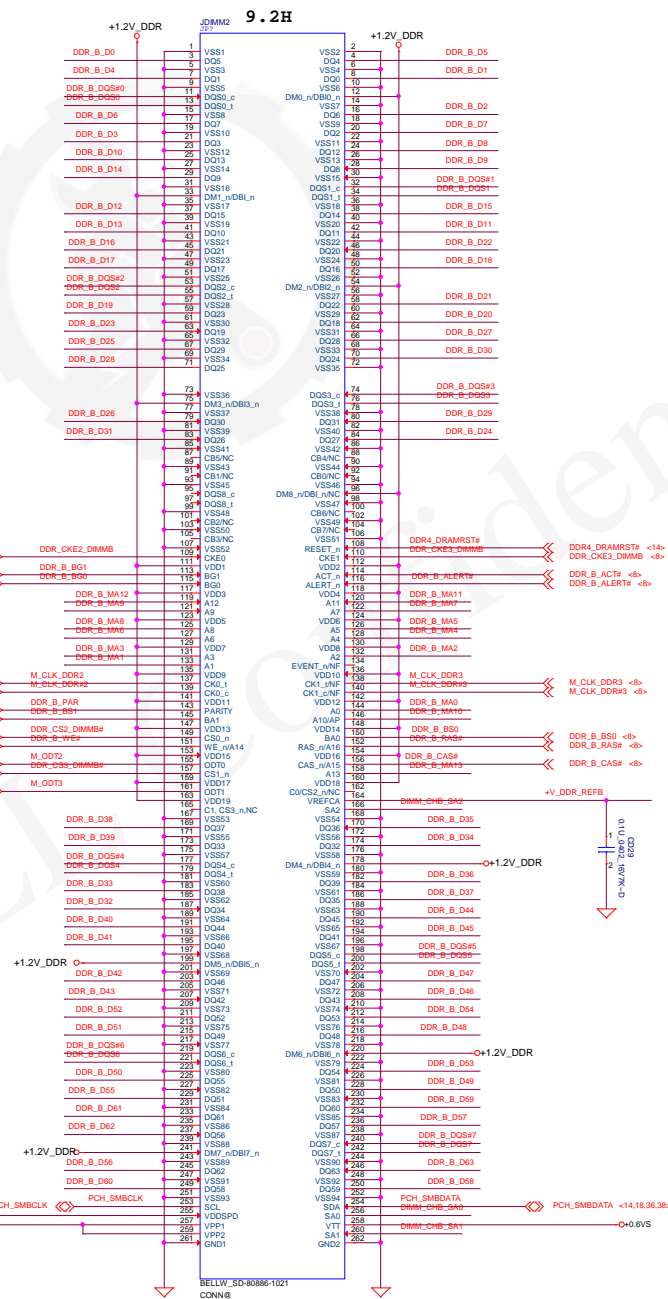
All VREF traces should  
have 10 mil trace width

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				Date	Wednesday, July 22, 2015
				Sheet	14 of 78



«B» DDR\_B\_DQ[0..63]  
«B» DDR\_B\_MA[0..15]  
«B» DDR\_B\_DQS[0..7]  
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All VREF traces should  
have 10 mil trace width

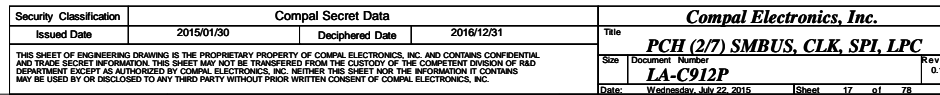
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				Sheet	15 of 78

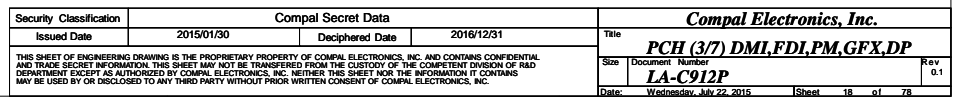


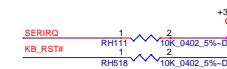
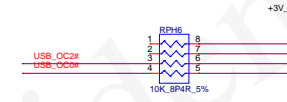
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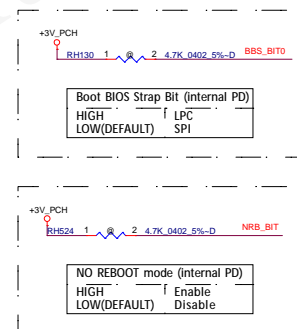
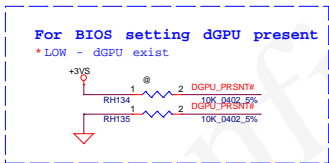
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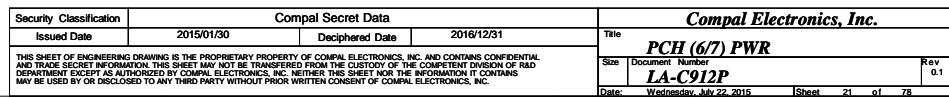


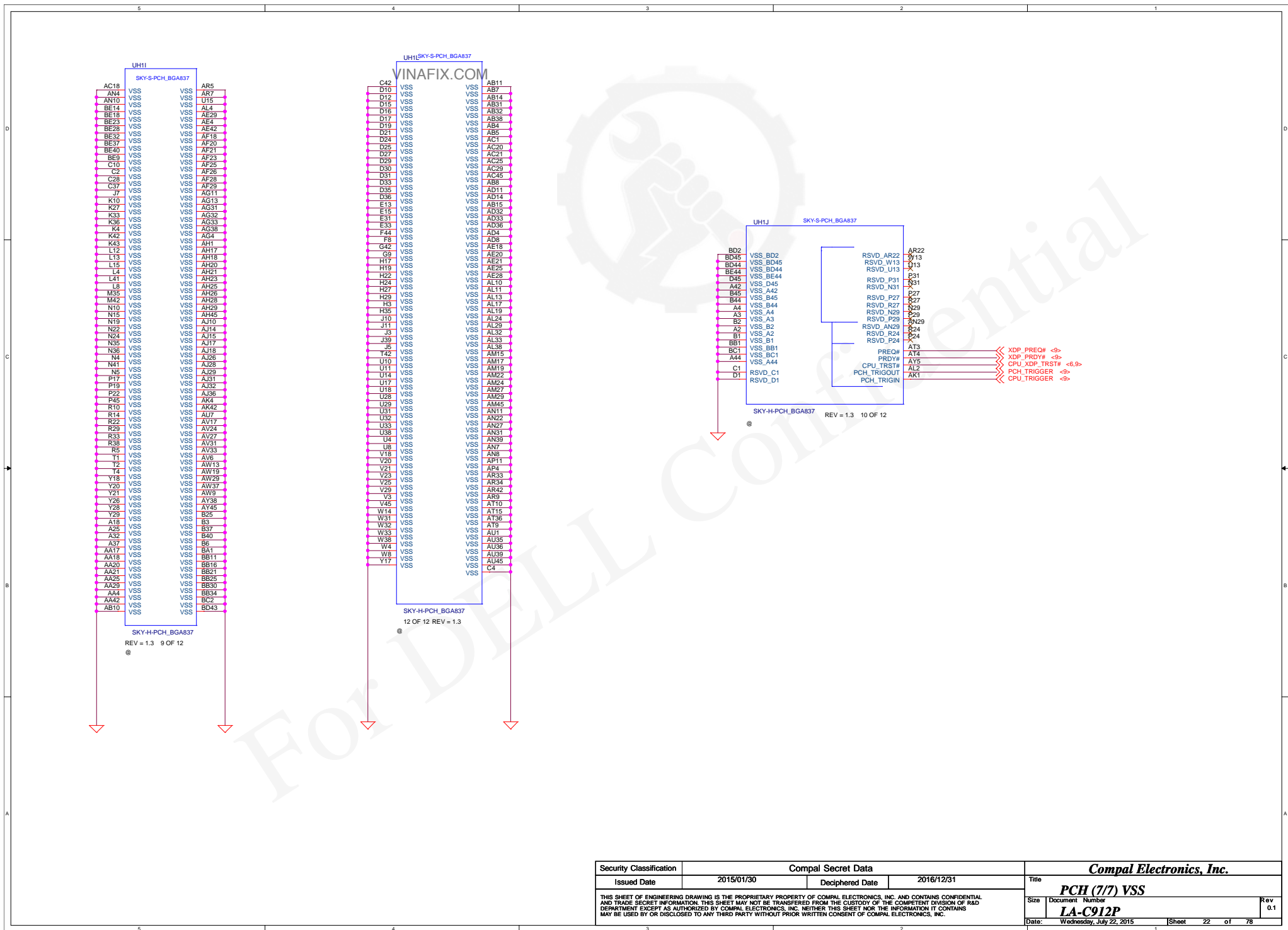


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				<b>LA-C912P</b>		
Date: Wednesday, July 22, 2015				Sheet	20	of 78





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				Date:	Wednesday, July 22, 2015
				Sheet	22 of 78
				Rev	0.1

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Date: Wednesday, July 22, 2015				Sheet 23 of 78

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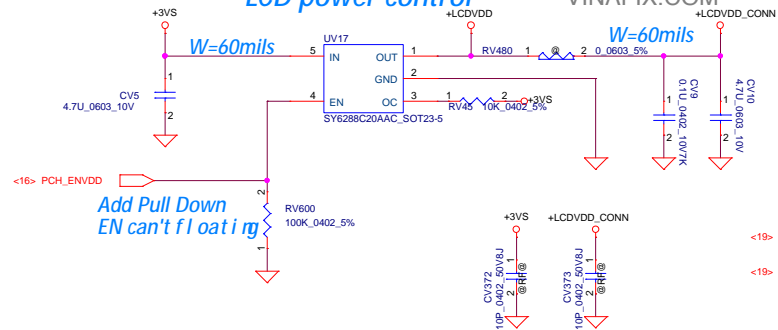
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				Document Number
				LA-C912P
				Rev
				0.1
Date: Wednesday, July 22, 2015				Sheet 24 of 78

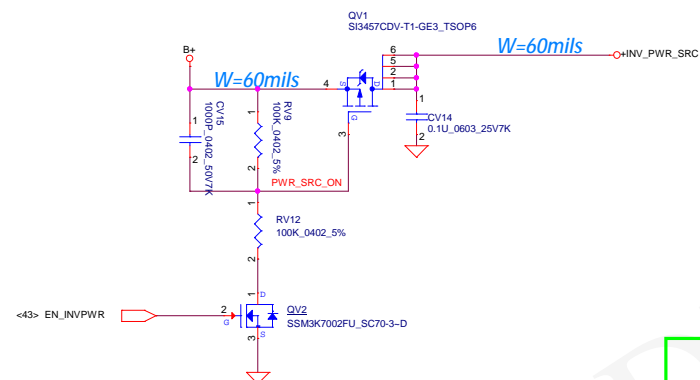


## LCD power control

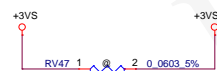
VINAFIX.COM



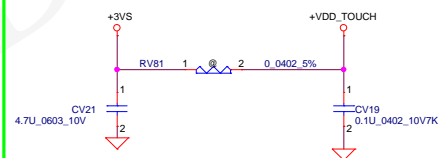
## LCD backlight power control



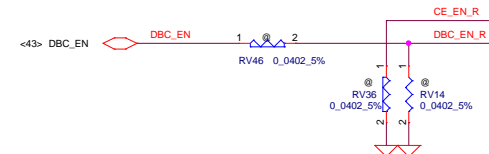
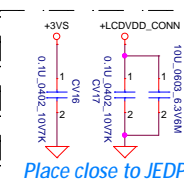
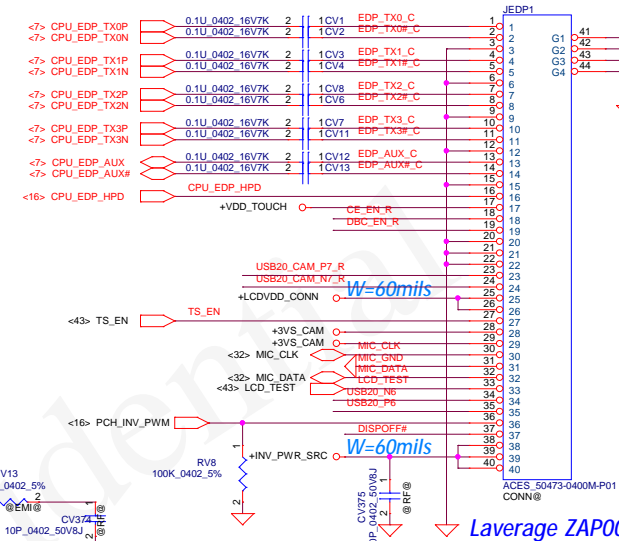
## Webcam power control



## Touch screen panel power control



## eDP connector



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				Rev	
				0.1	
				Date: Wednesday, July 22, 2015	
				Sheet 25 of 78	

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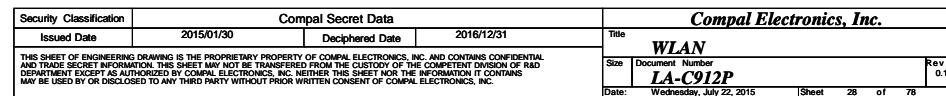


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For DELL Confidential

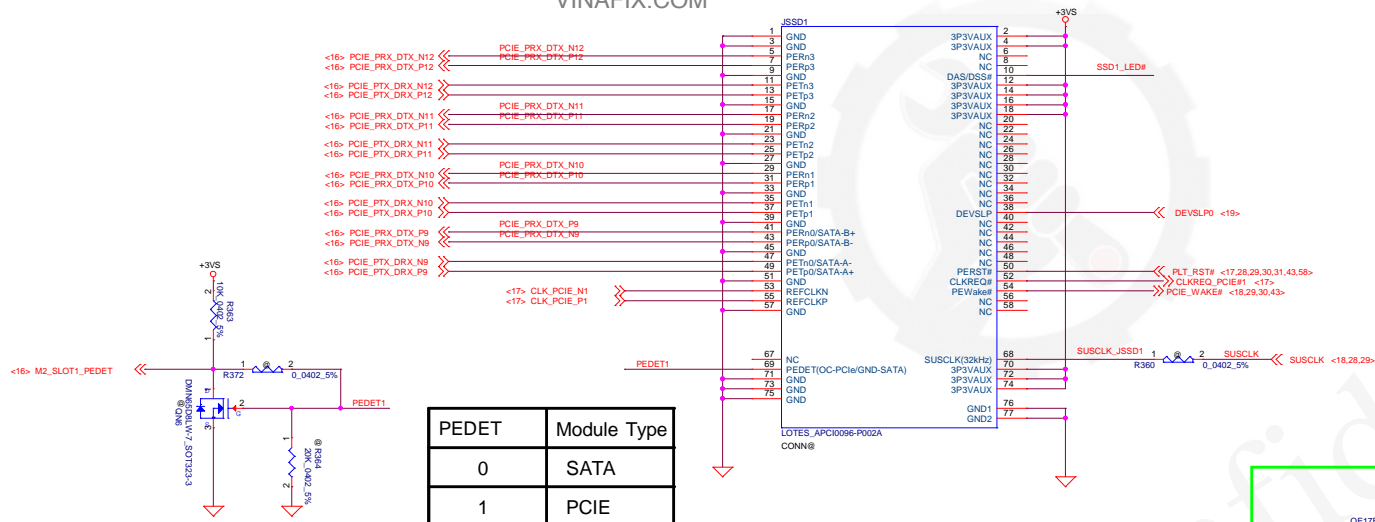
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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					3D Camera
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				Date:	Wednesday, July 22, 2015
				Sheet	26 of 78
				Rev	0.1



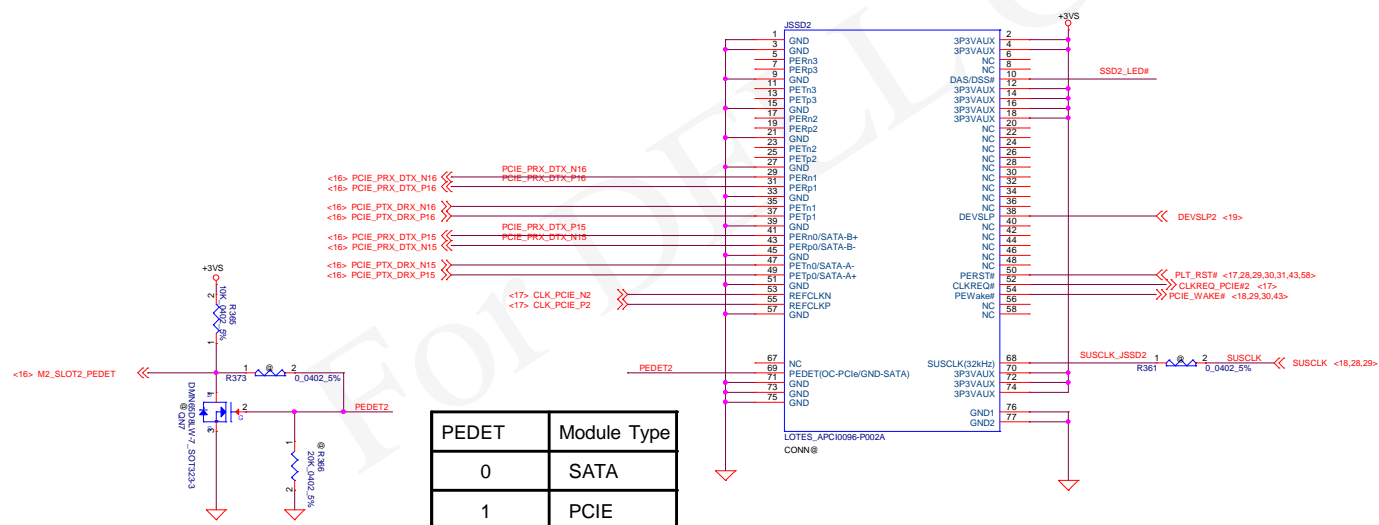


# SSD NGFF slot\_1 Key M

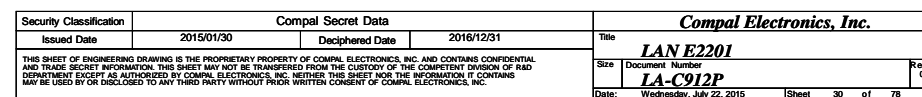
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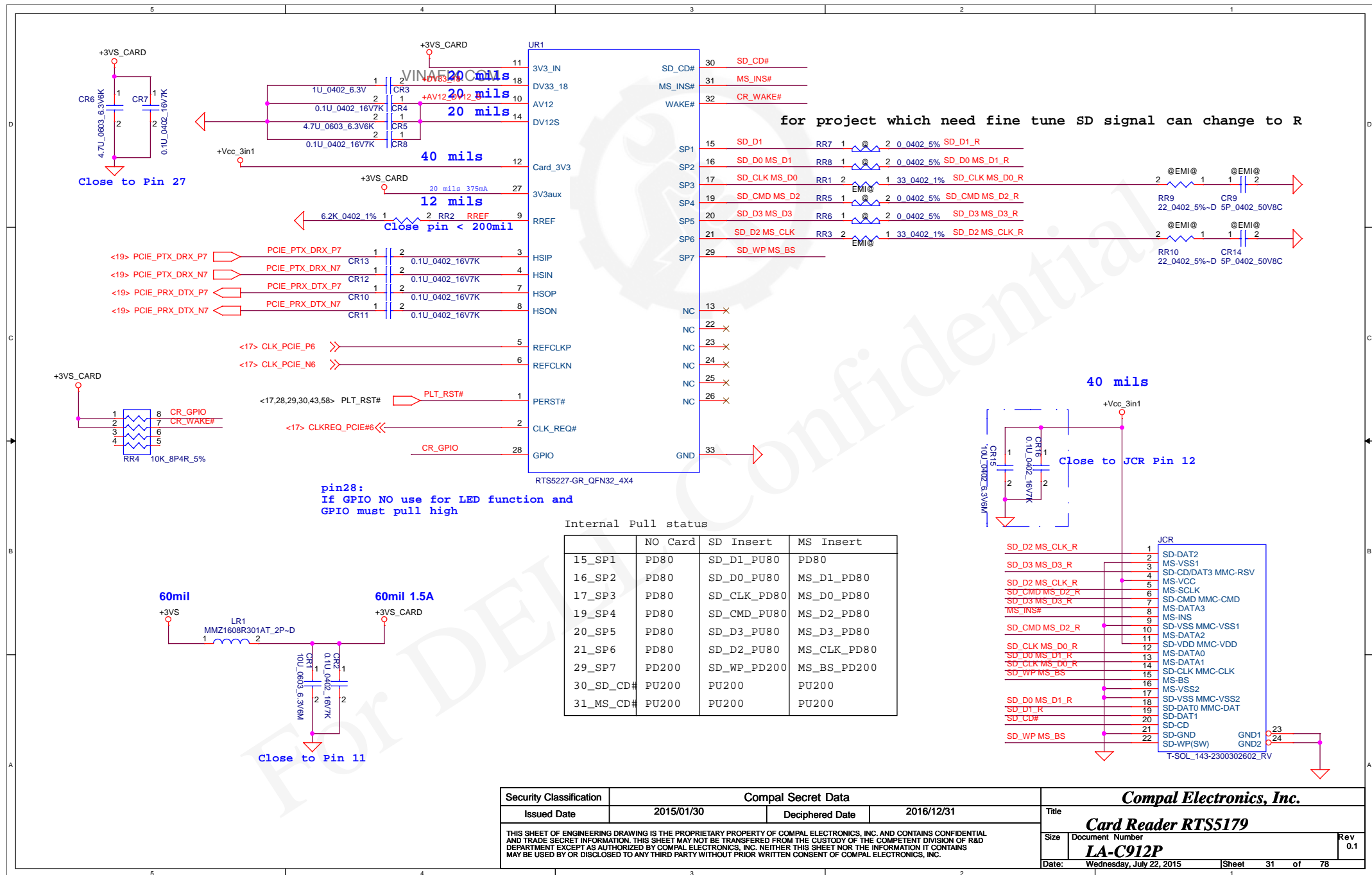


# SSD NGFF slot\_2 Key M

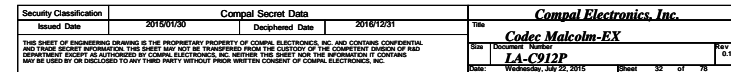


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Size	Document Number	Sheet	29 of 78	Rev 0.1
Date: Wednesday, July 22, 2015				





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Size	Document Number	Rev			0.1
Date:	Wednesday, July 22, 2015	Sheet	31	of	78





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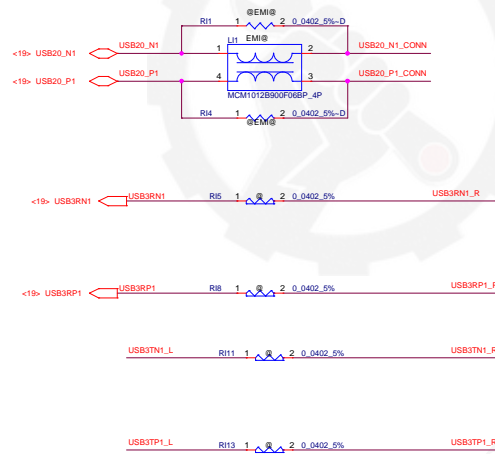
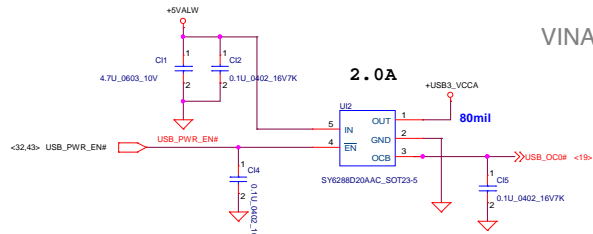


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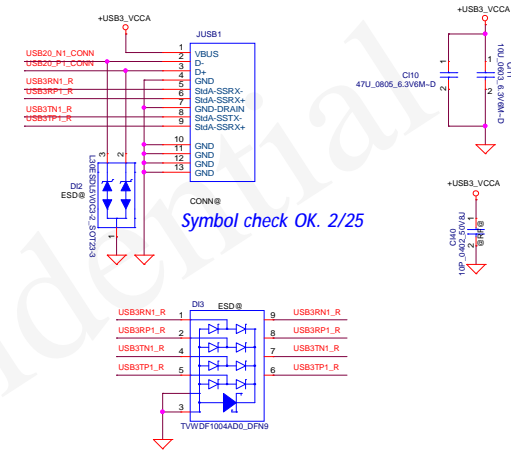
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				Rev
				0.1
Date: Wednesday, July 22, 2015				Sheet 33 of 78

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JUSB1

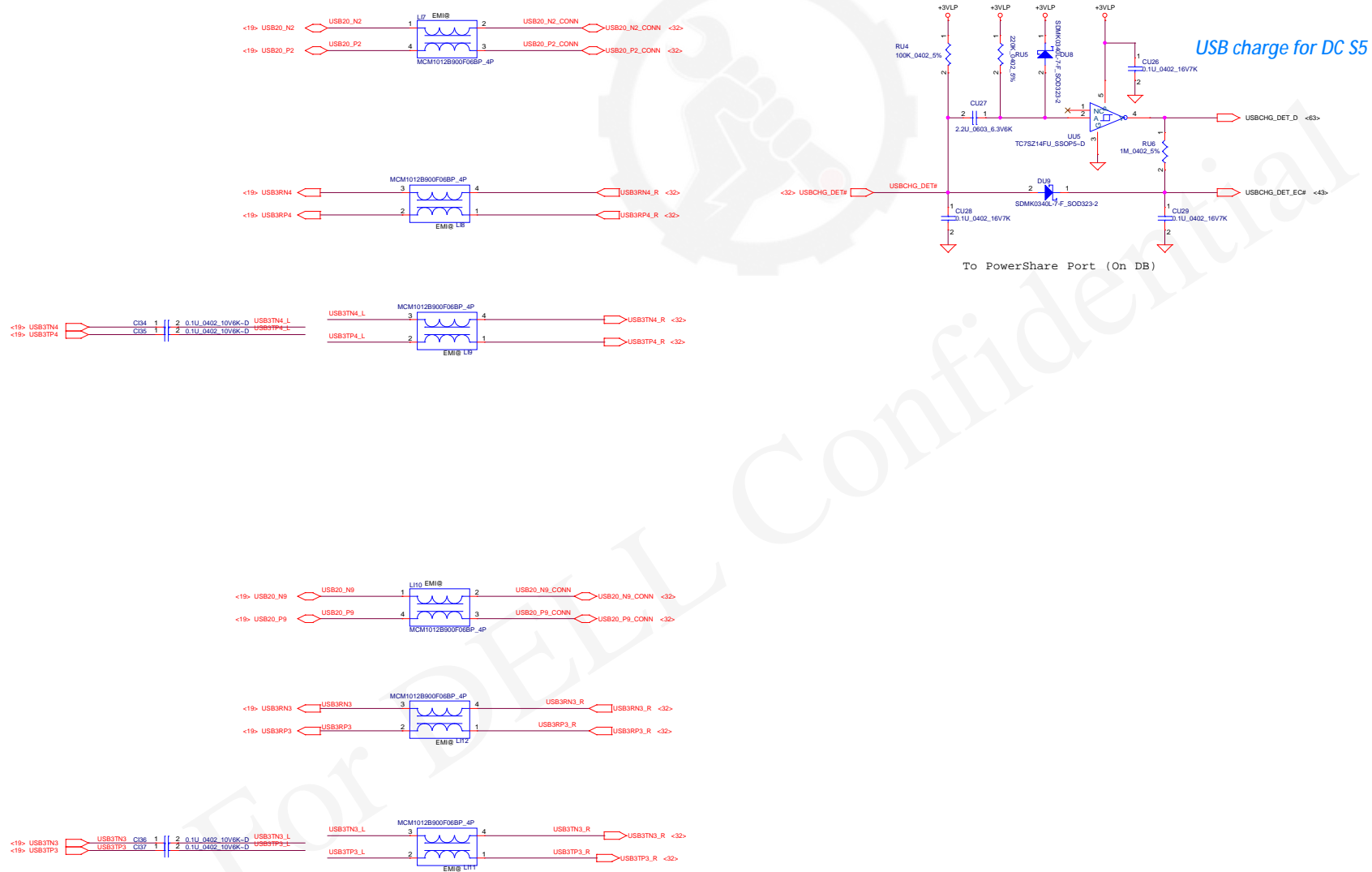
On MB (Right Side)



JUSB2 change to TypeC

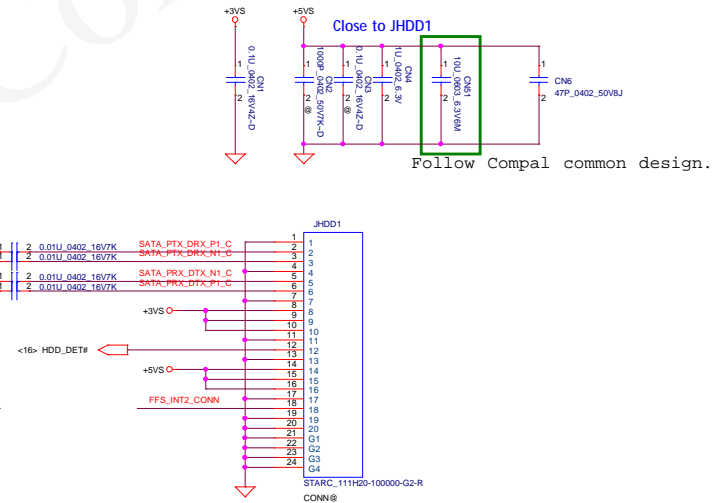
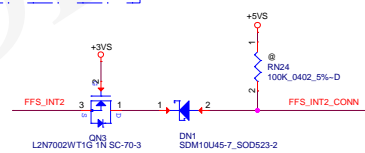
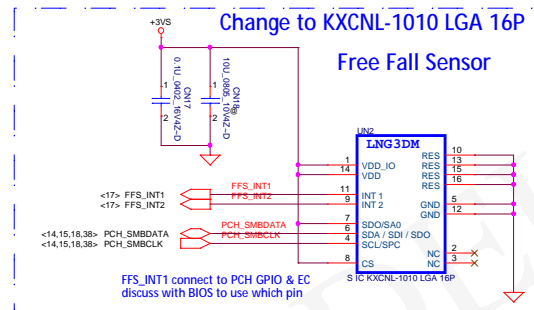
Security Classification	Compal Secret Data		Title	
Issued Date	2015/01/30	Deciphered Date	2016/12/31	2016/12/31
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Compal Electronics, Inc.				LA-C912P
USB 3.0/2.0 x2 (left side)				34 of 76
Date: Wednesday, July 22, 2015				1Sheet

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Date: Wednesday, July 22, 2015				Sheet 35 of 78

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				HDD/ODD
				Size
				Document Number
				LA-C912P
				Rev
				0.1
				Date
				Wednesday, July 22, 2015
				Sheet
				36 of 78

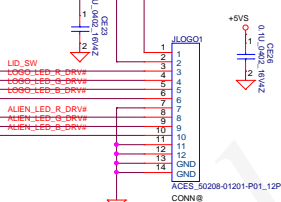
Security Classification		Compal Secret Data		Title	
Issued Date	2015/01/30	Deciphered Date	2016/12/31	<b>ELC (1)</b> <b>ELC Number</b> <b>LA-C912P</b>	
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Date:				Wednesday, 12/22/2015	Sheet 37 of 76

## MAX7313 change to TI TLC59116F PWM expander

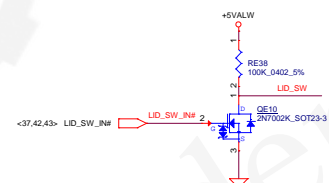
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## Power LED

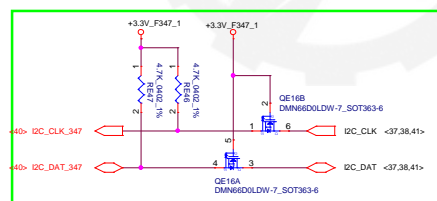
W=20mils



## Logic up LED board



## For IND/TP/HDD/PWR



To Hot Key

## For TouchPAD

## Power ON Circuit

## ON/OFF switch

ON/OFF switch power button  
Bottom Side pop only before MP

## Touchpad LED circuit

Change Symbol OK  
2/18 -Tarry

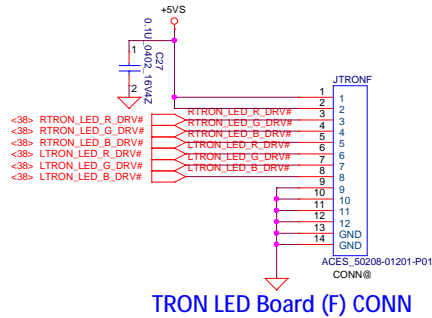
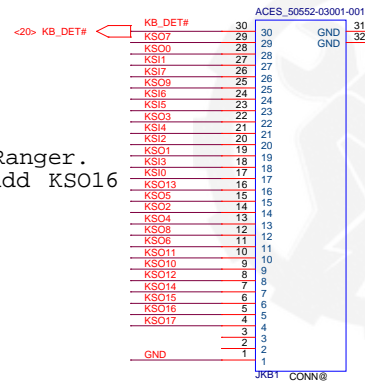
Security Classification		Compal Secret Data		Title	
Issued Date	2015/01/30	Deciphered Date	2016/12/31	ELC (2)/TP/PWR SW	
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				Sheet	LA-C912P
				Date	Wednesday, July 22, 2015
				Sheet	38 of 76

## INT\_KBD Conn.

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KSII[0..7] <43>  
KSO[0..17] <43>

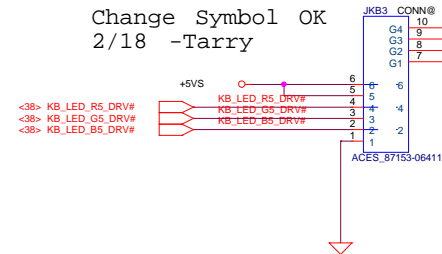
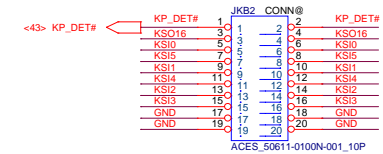
Net follow Ranger.  
Only Pin26 add KSO16



TRON LED Board (F) CONN

Hot Key Conn.  
PWM

Change Symbol OK  
2/18 -Tarry

Hot Key Conn.  
Key Pad

Compal Electronics, Inc.			
Title			
KB/HotKey conn			
Size	Document	Number	Rev
		LA-C912P	0.1
Date:	Wednesday, July 22, 2015	Sheet	39 of 78

1/28 ADD

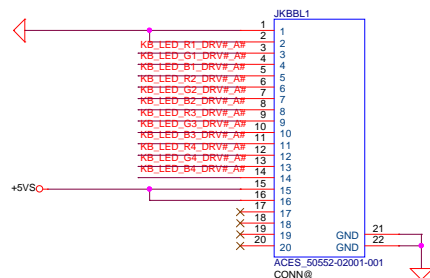
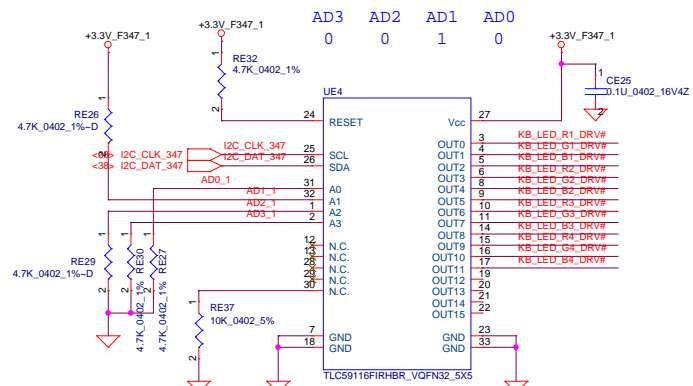
+5VS RE104 1 2 0.0603.5%  
 +3VS RE105 1 2 0.0603.5%

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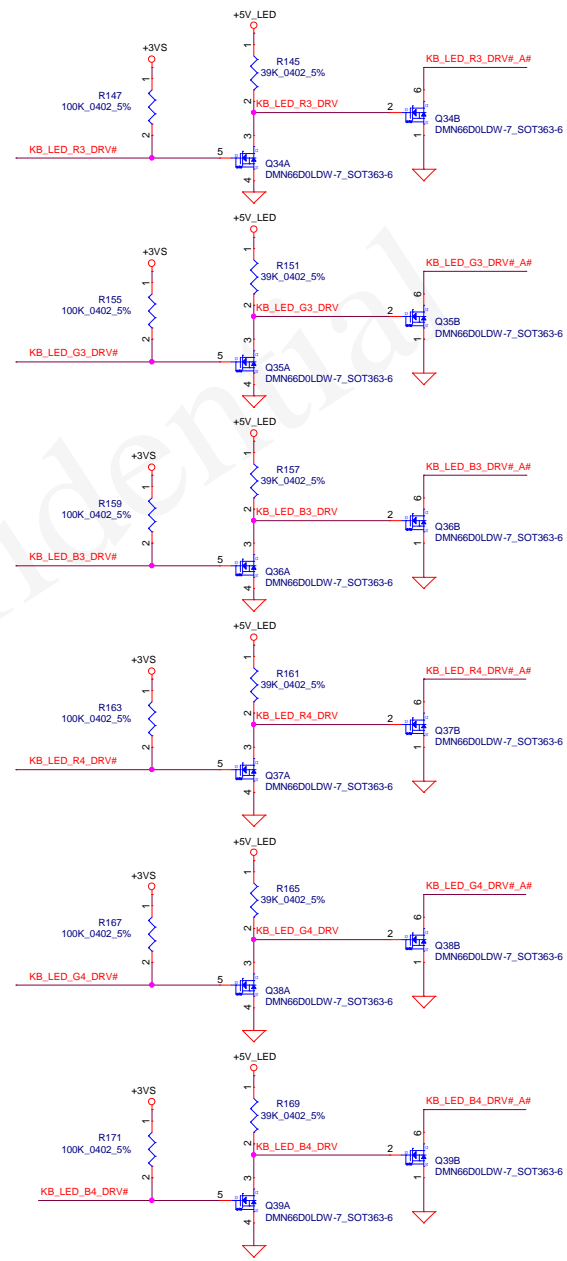
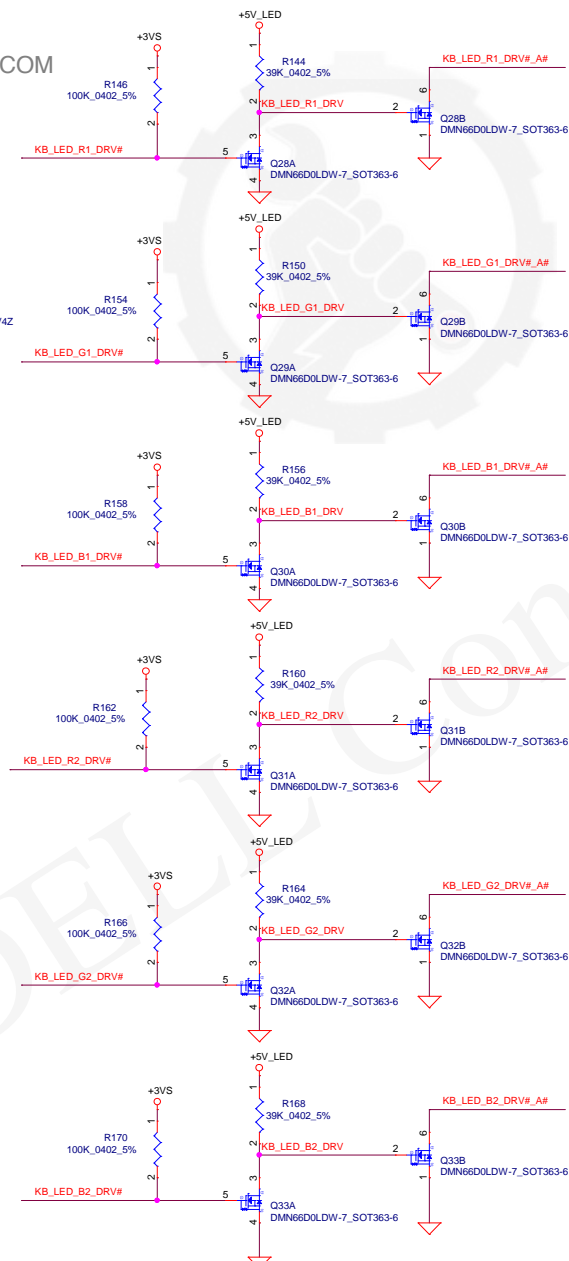
## K/B Backlight

AD3 AD2 AD1 AD0

0 0 1 0



KB BL LED

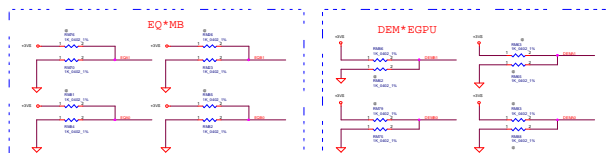
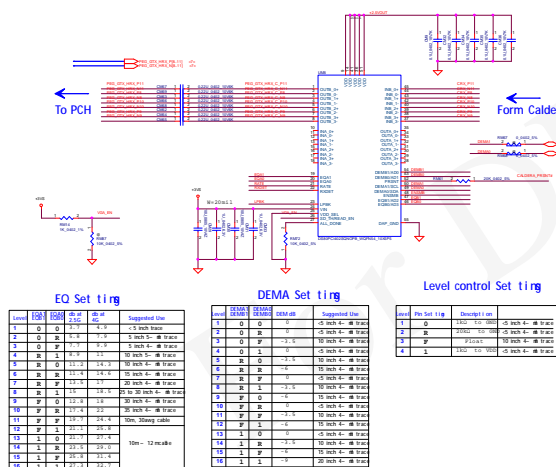
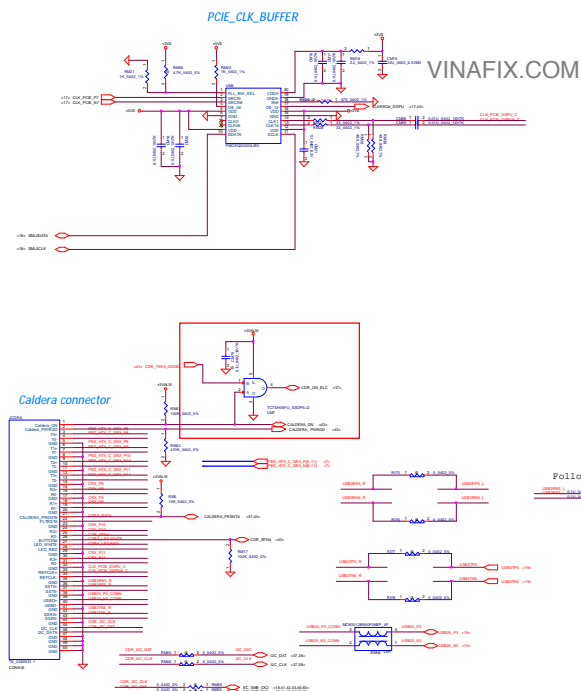


Compal Electronics, Inc.

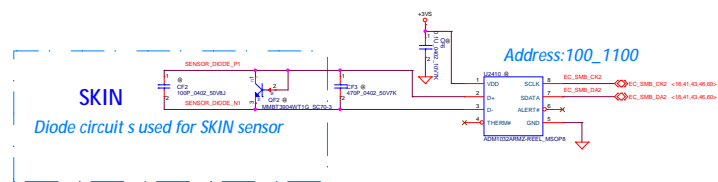
Title	ELC(3)		
Size	Document	Number	Rev
	LA-C912P		0.1
Date:	Wednesday, July 22, 2015	Sheet	40 of 78



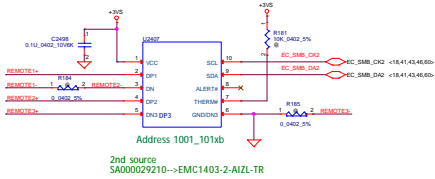
EC# P IN  
PCI\_SMLCK  
PCI\_SMLDAT  
USB\_PWR\_EN#  
DOCKING\_LED\_ON#  
DOCKING\_LED\_OFF#  
DOCK\_PSID  
DOCK\_ACIN  
DOCK\_EN  
PRSNTR\_R



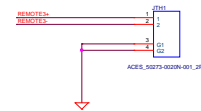
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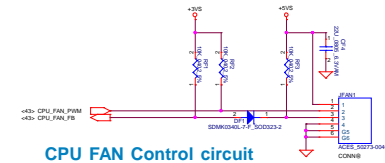
Fintek thermal sensor-&gt; CPU core, DIMM



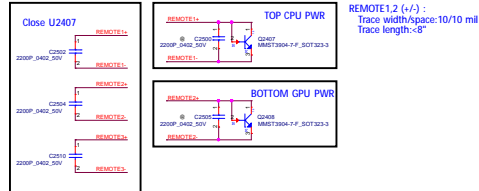
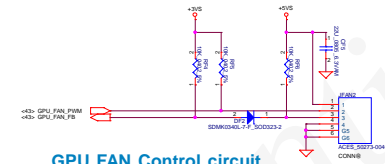
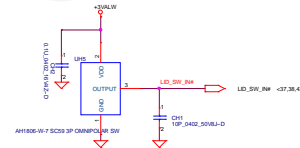
Thermal Board for SSD



CPU FAN Control circuit



GPU FAN Control circuit

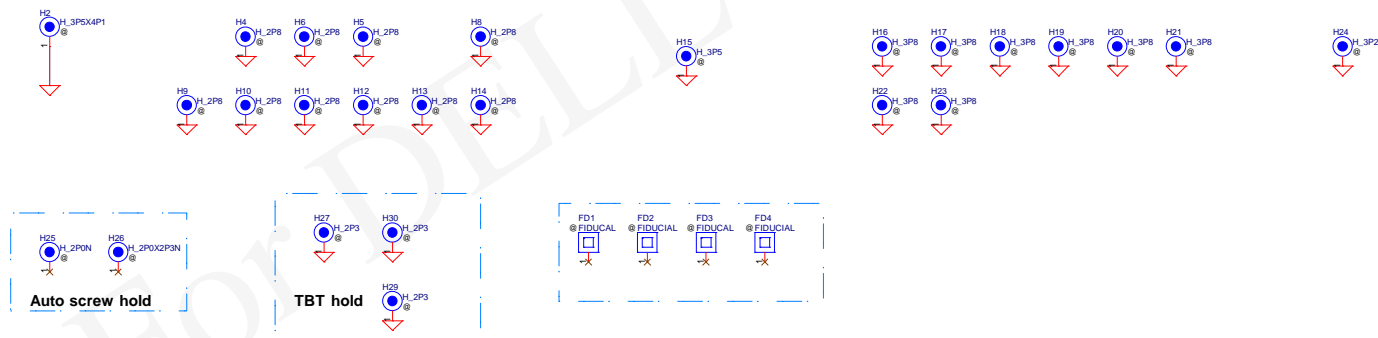
Lid Switch  
(Hall Effect Switch)

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Title			FAN/TP/PWR SW
Size			LA-C912P
Date			Wednesday, July 21, 2015



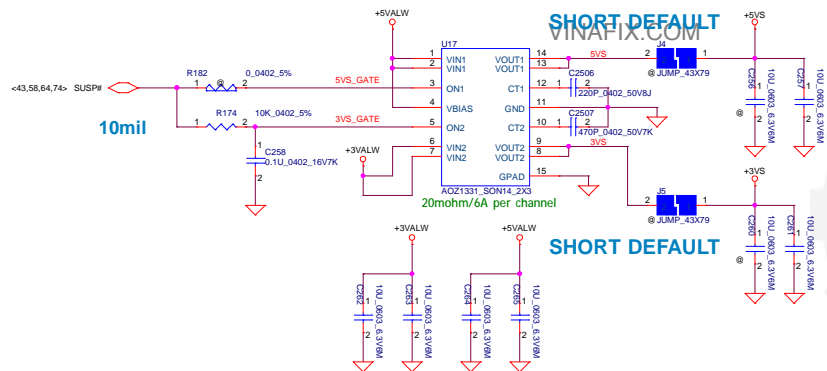
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## Screw Hole

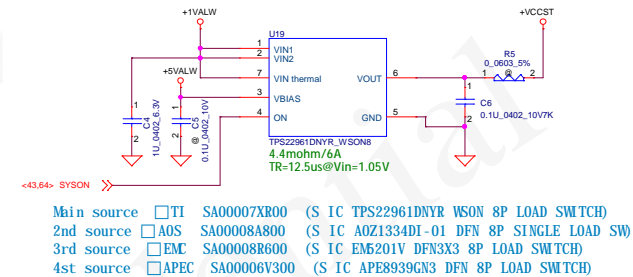


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				Document Number
				LA-C912P
				Rev
				0.1
				Date
				Wednesday, July 22, 2015
				Sheet
				44 of 78

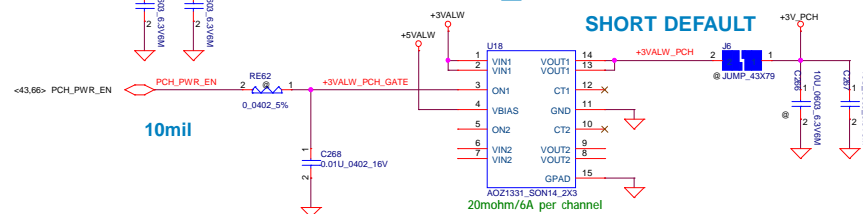
## +5VS and +3VS switch



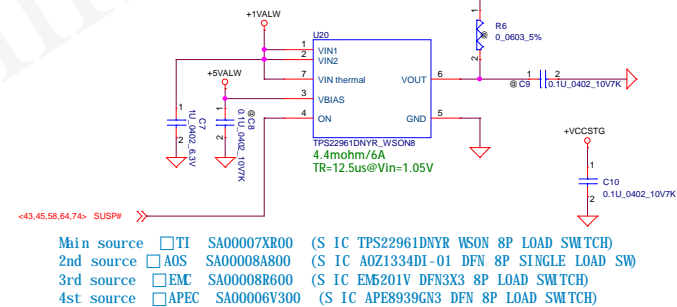
## +VCCST Load Switch



## +3VALW\_PCH switch

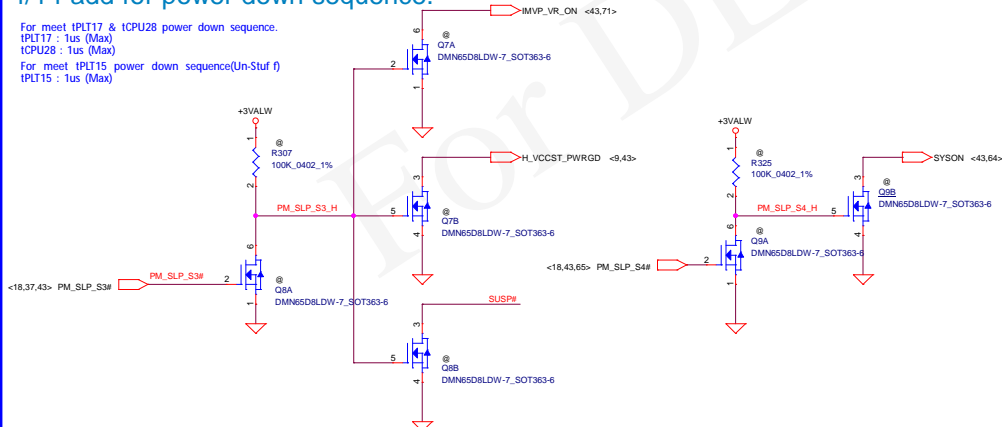


## +VCCSTG source

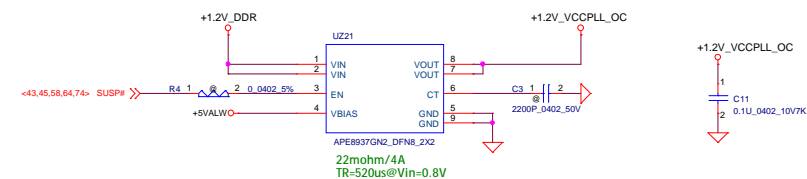


## 4/14 add for power down sequence.

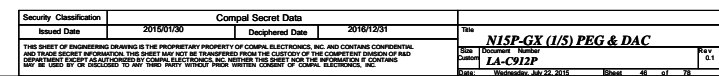
For meet tPLT17 & tCPU28 power down sequence.  
 tPLT17 : 1us (Max)  
 tCPU28 : 1us (Max)  
 For meet tPLT15 power down sequence(Un-Stuf f)  
 tPLT15 : 1us (Max)

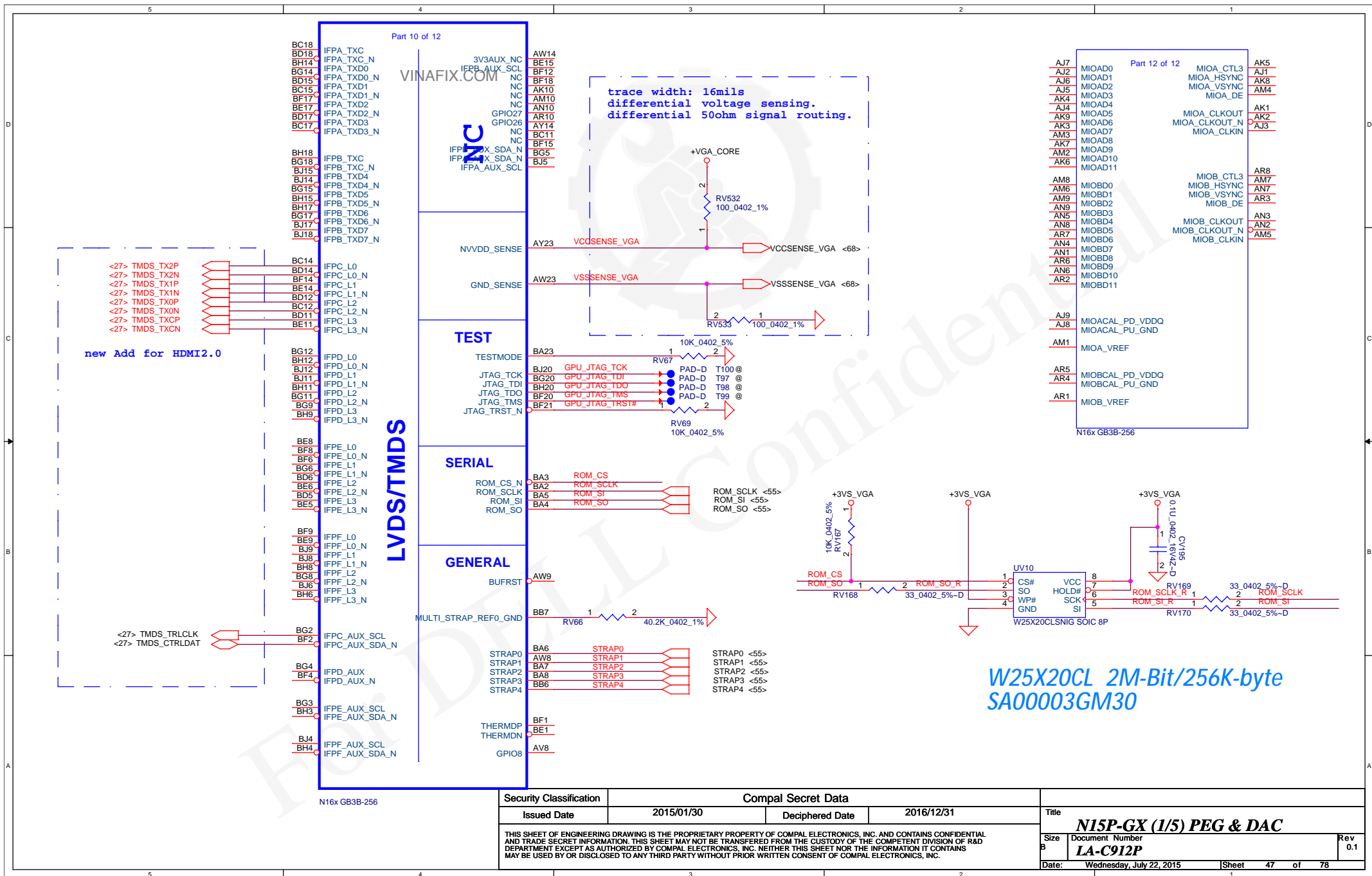


## +1.2V\_VCCPLL\_OC

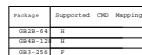


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				LA-C912P	Rev 0.1
				Date	Wednesday, July 22, 2015
				Sheet	45 of 78









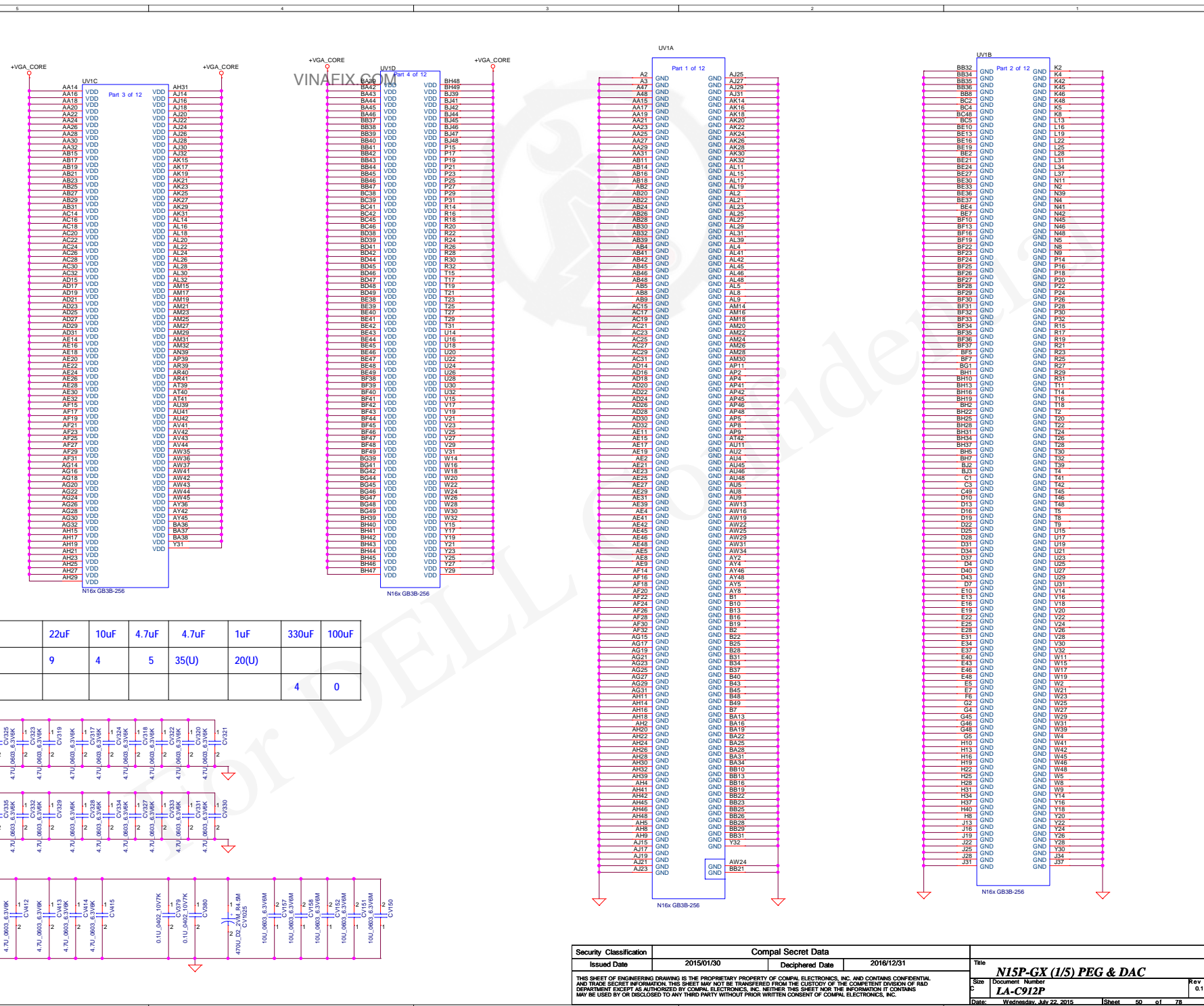
Node #	5...11	Node #	12...63
OS025	OS*	OS016	OS*
OS026	A3_A3	OS017	A3_A3
OS027	A2_BA0	OS018	A2_BA0
OS028	A4_BA2	OS019	A4_BA2
OS029	A1_A8	OS020	A5_A1
OS030	WE*	OS021	WE*
OS031	A7_A8	OS022	A7_A8
OS032	A6_A11	OS023	A4_A11
OS033	A10_A12	OS024	A5_A12
OS034	A12_BF0	OS025	A12_BF0
OS035	A8_A10	OS026	A8_A10
OS036	A1_A8	OS027	A1_A8
OS037	BA5*	OS028	BA5*
OS038	BF0*	OS029	BF0*
OS039	CL1*	OS030	CL1*
OS040	CA5*	OS031	CA5*
OS041	OS017	OS032	OS017
OS042	OS018	OS033	OS018
OS043	OS019	OS034	OS019
OS044	OS020	OS035	OS020
OS045	OS021	OS036	OS021

Node #	ASD	ASD	ASD	ASD
Node #	ASD	ASD	ASD	ASD
CM01	CR1*	CM016	CR1*	
CM02	RST*	CM018	RST*	
CM03	RST*	CM019	RST*	
CM04	AT_A9	CM020	AT_A9	
CM05	AT_A10	CM021	AT_A10	
CM06	AT_A12	CM022	AT_A12	
CM07	AT_A13	CM023	AT_A13	
CM08	AT_A11	CM024	AT_A11	
CM09	AT_A8	CM025	AT_A8	
CM10	WE*	CM026	WE*	
CM11	AS_BA1	CM027	AS_BA1	
CM12	AS_BA2	CM028	AS_BA2	
CM13	AS_BA0	CM029	AS_BA0	
CM14	AS_BA3	CM030	AS_BA3	
CM15	CP*	CM031	CP*	
CM16	NO_USED			
CM17	NO_USED			
CM34	Dnslogp			
CM35	Dnslogp1			

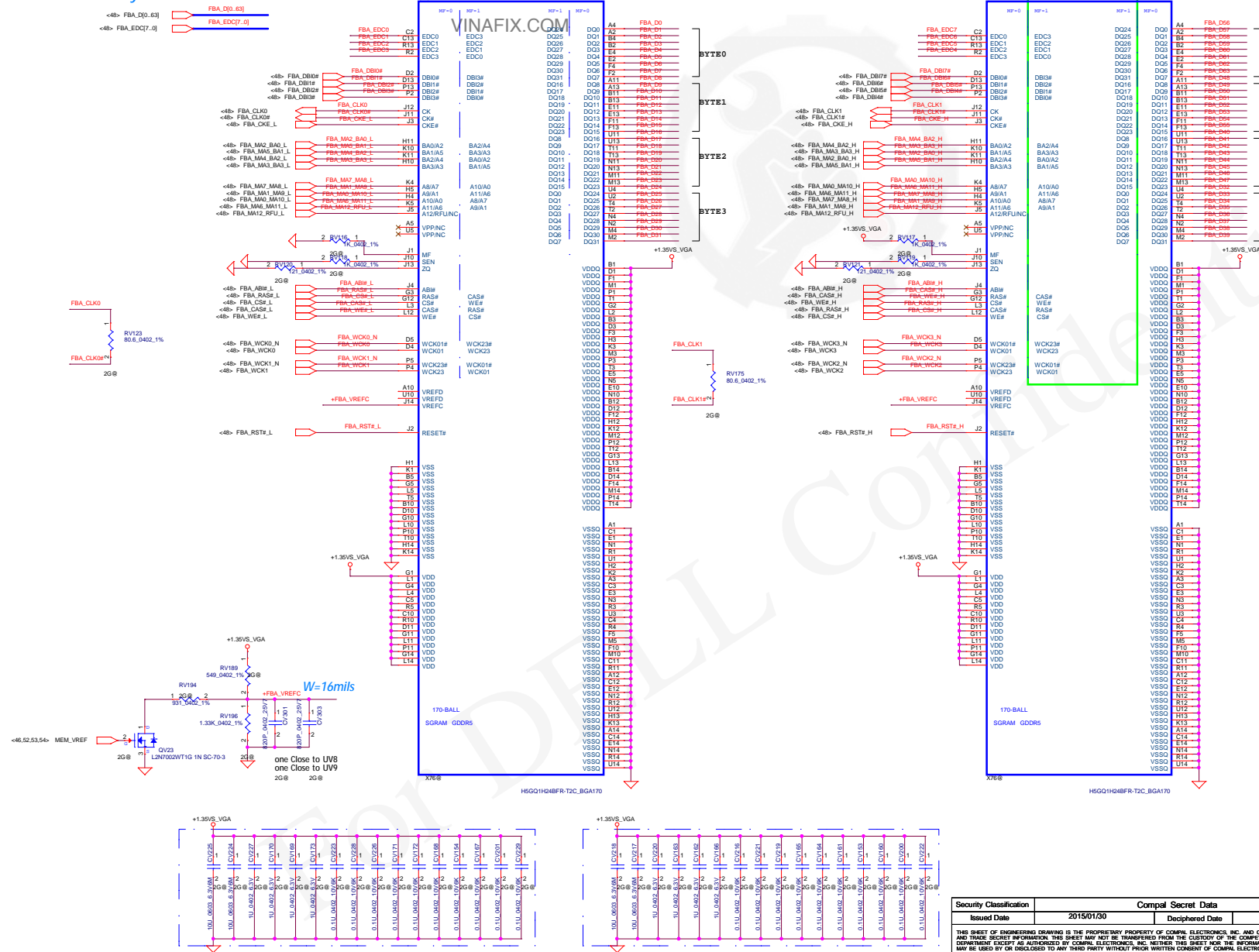
Security Classification	Compul Secret Data		File
Issued Date	2010/12/31	Deciphered Date	
<p>THE ISSUED OF DISSEMINATED IS THE PROPRIETARY PROPERTY OF CANAL, ELECTRONICS, INC AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE REPRODUCED FROM THE CUSTODY OF THE COMPANY WITHOUT THE WRITTEN PERMISSION OF CANAL ELECTRONICS, INC. ANY REPRODUCTION OF THIS SHEET WITHOUT THE WRITTEN PERMISSION OF CANAL ELECTRONICS, INC. IS PROHIBITED.</p>			<p><b><u>NISP-GX (5/5) POWER/ GND</u></b></p> <p>Doc Number</p> <p><b><u>LA-C912P</u></b></p>





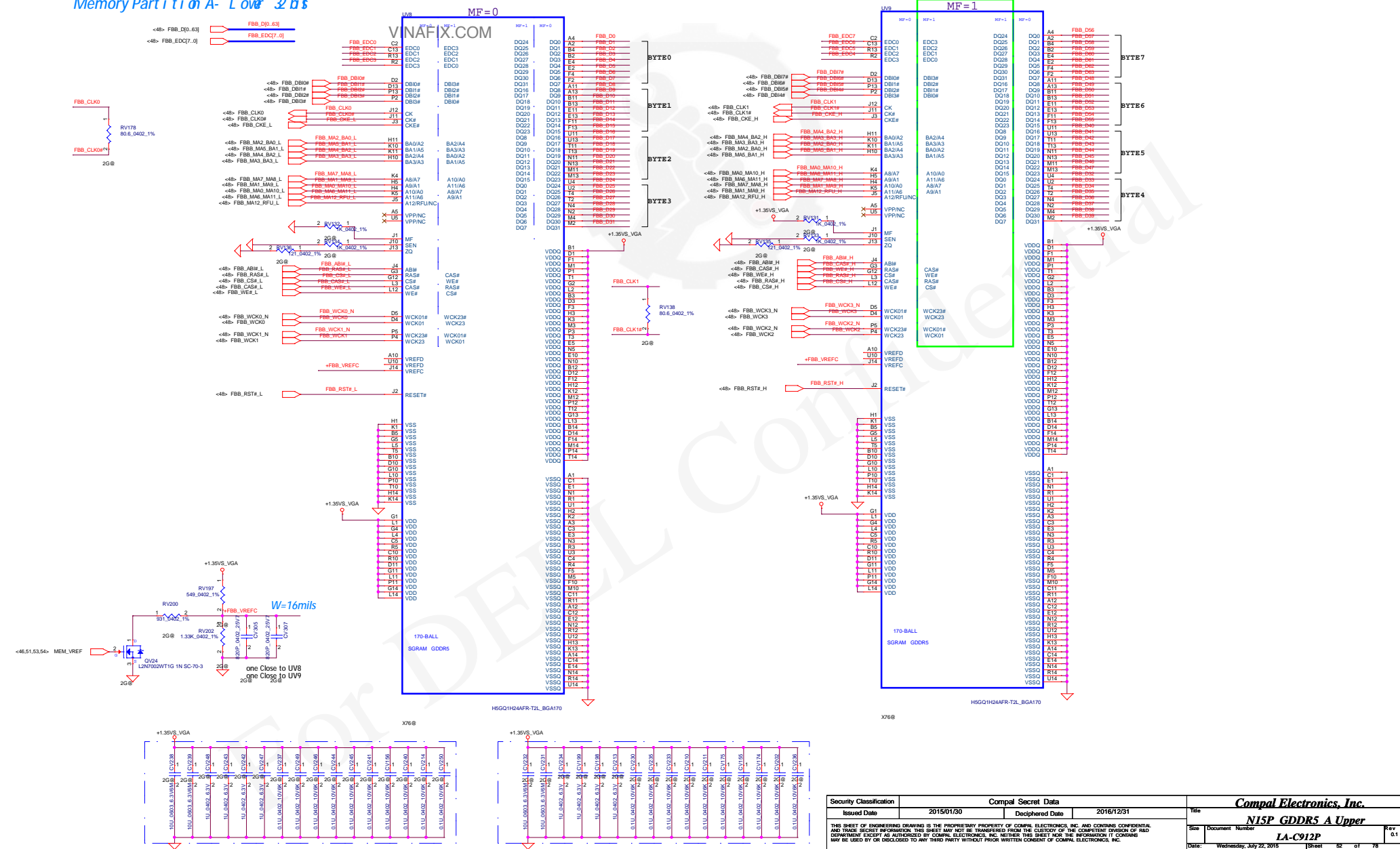


### Memory Partition A- L over 32 bits

$$MF=0$$


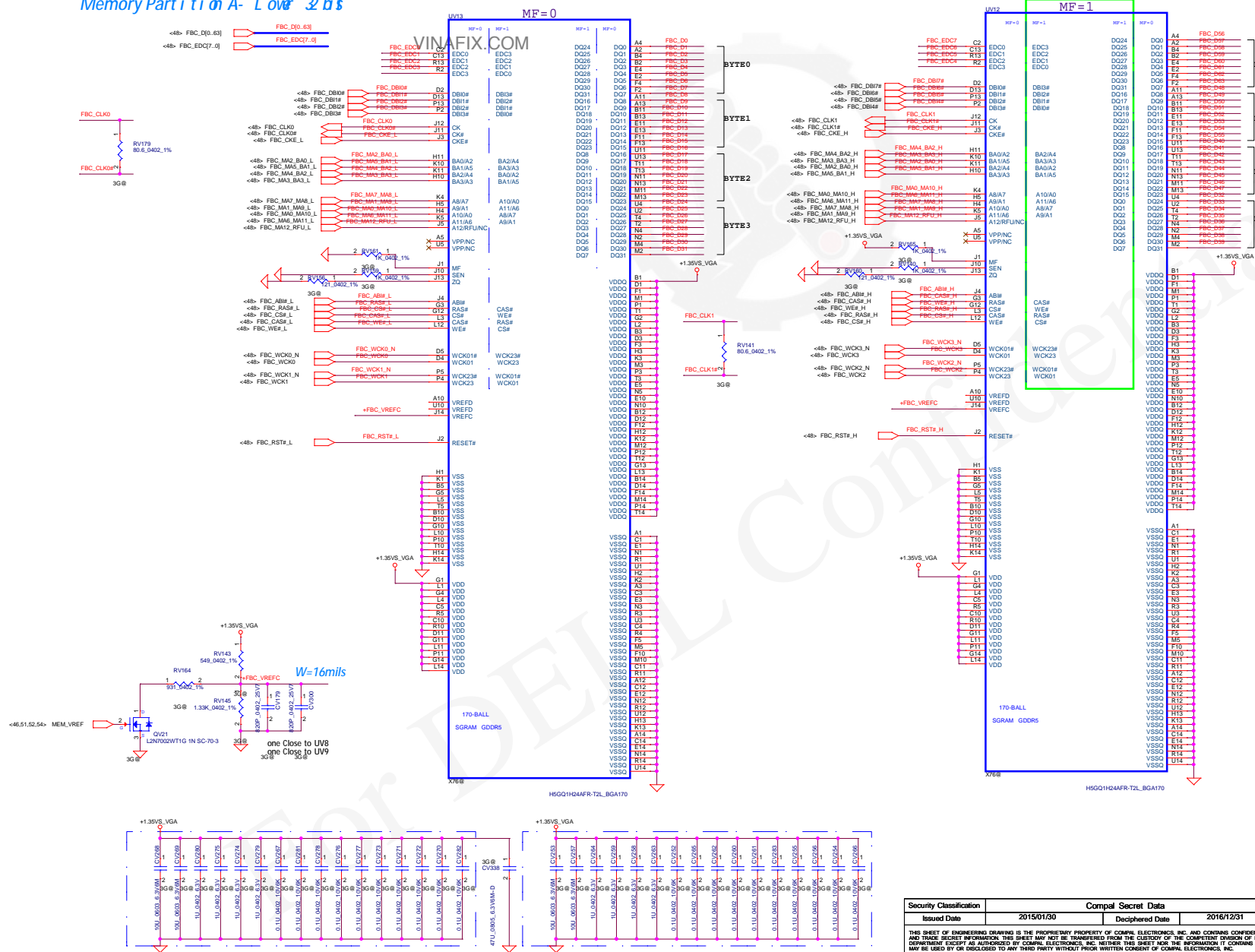
Security Classification	Compul Secret Data		<b>Compul Electronics, Inc.</b>	
Issued Date	2015/01/30	Deciphered Date	2016/2/23/1	Title
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			<b>N1SP GDDR5 A Lower</b> <b>LA-C912P</b>	
			Date	Wednesday, July 22, 2015
			Sheet	51 of 78

Memory Partition A- L over 32 bits



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Issued Date	2015/01/30	Deciphered Date	2016/12/31	N15P GDDR5 A Upper		
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					LA-912P	0.1
Date:	Wednesday, July 22, 2015		Sheet	82	of	78

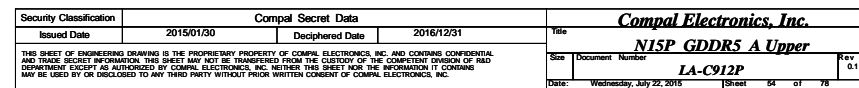
Memory Partition A- Lower 32 bits

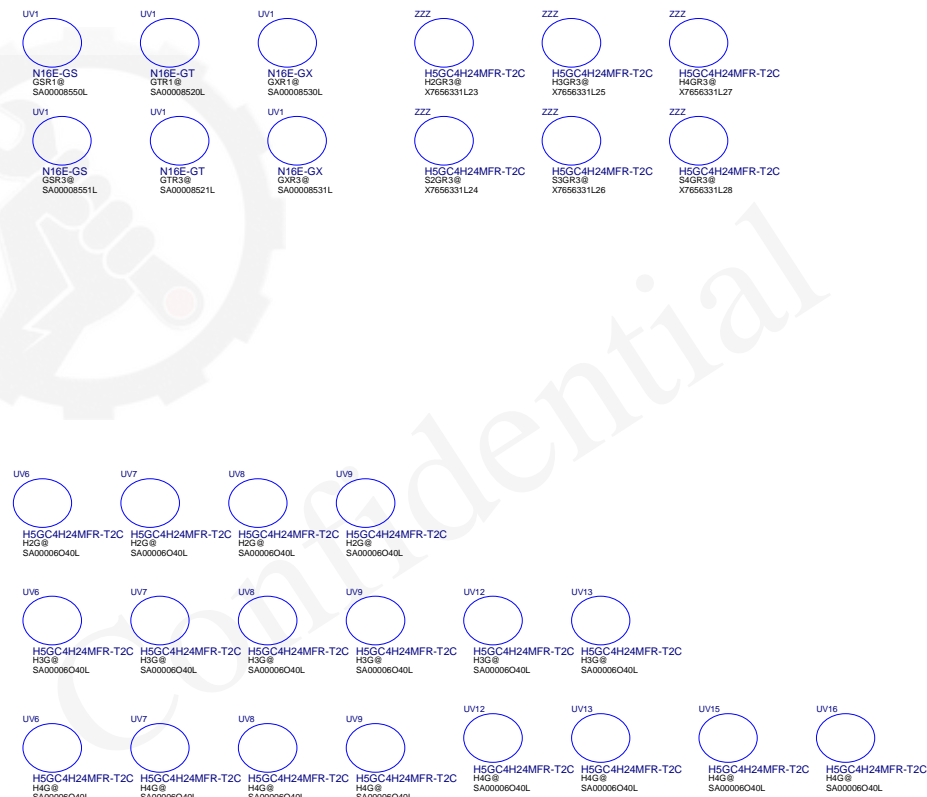


Security Classification	Compul Secret Data		<b>Compul Electronics, Inc.</b> <b>NISP GDDR5 A Upper</b>	
Issued Date	2015/01/30	Deciphered Date	2016/12/31	Title <b>NISP GDDR5 A Upper</b> <b>LA-912P</b>
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Date:			Wednesday, July 22, 2015	[Print] 53 of 78



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```

PCI_DEVID
SUB_VENDOR
0- w/o dGPU ROM
1-w/ dGPU ROM
FB[1:0]
0-Reserved
1-Reserved
2-256M
3-Reserved
VGA_DEVICE
0- Non-permarty 3D
1-
SMB_ALT_ADDR
0-0x9E
1-0x9C(Multi-l GPU)
PEX_PLL_EN_TERM
0-Disable
1-Enable
3GIO_PADCFG
0100-GEN1/GEN2
0000-GEN3
PCIe_MAX_SPEED
0-booting to PCIe
1-booting to PCIe
PCIe_SPEED_CHNAG
0-Disable PCIe Gen
1-Enable PCIe Gen

```

	PU to 3V3	PD to GND
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

Physical Strapping pin	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	PCI_DEVID[4]	SUB_VENDER	PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SO	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SI	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	3GIO_CFG[3]	3GIO_CFG[2]	3GIO_CFG[1]	3GIO_CFG[0]
<b>STRAP2</b>	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	RESERVED	PCIE_SPEED_CHNAGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Security Classification		Compal Secret Data		Title	
Issued Date	2015/01/30	Deciphered Date	2016/12/31	<b><i>NISP-GX (1/5) PEG &amp; DAC</i></b> Subj: <b><i>CONFIDENTIAL</i></b> <b><i>LA-C912P</i></b>	
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Date:	<i>Wednesday, July 22, 2015</i>	Sheet	55	of	78

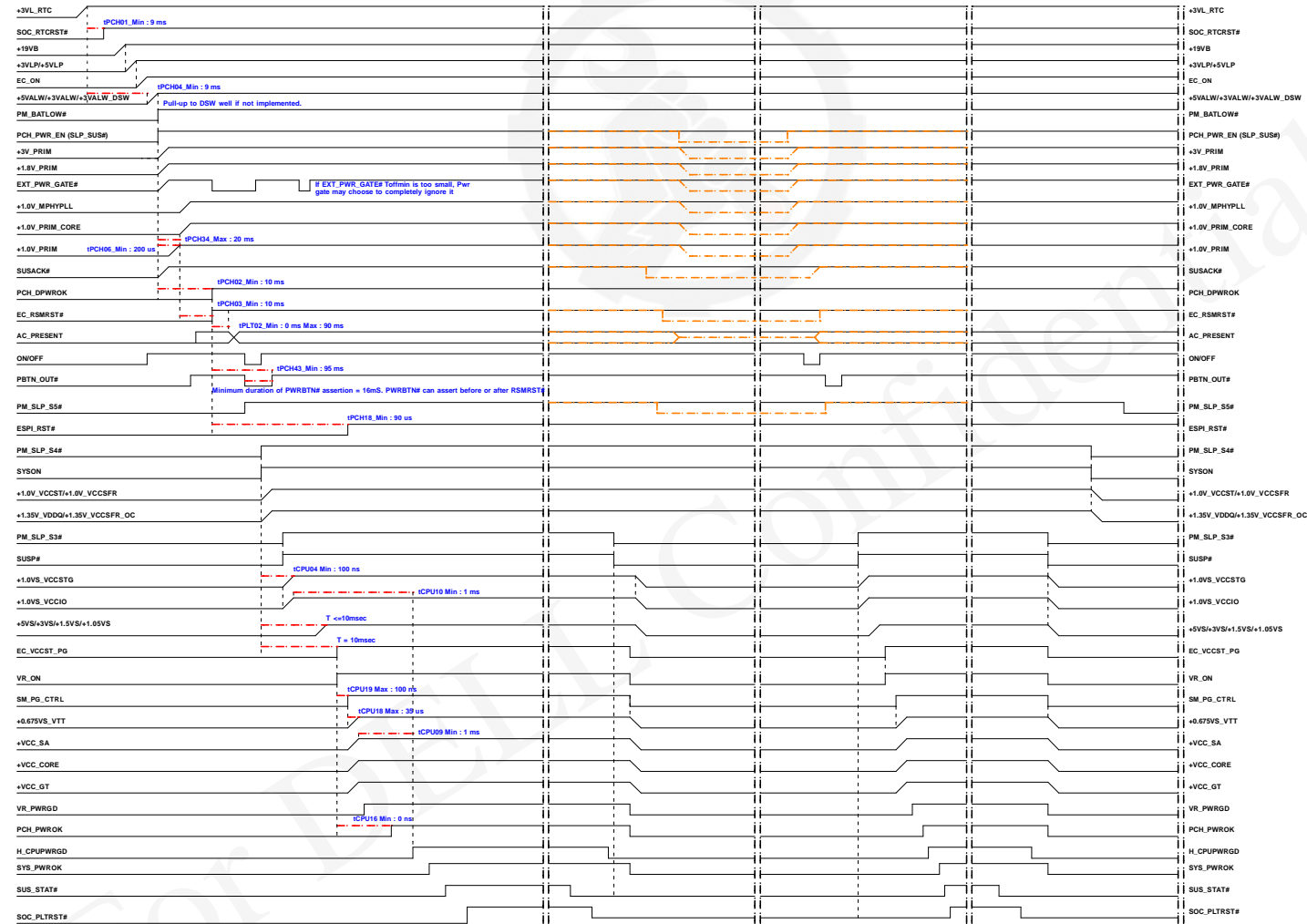
[AAX06-PWR Sequence\_SKL-H 4+4\_DDR4\_Volume\_NON CS]

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G3->S0

S0->S3/DS3

S0/DS3->S0

S0->S5



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Issued Date	2016/07/26	Disciplined Date	2016/10/31	Doc	Power Sequence
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				Author	LA-CHOP
				Check	2016/10/31



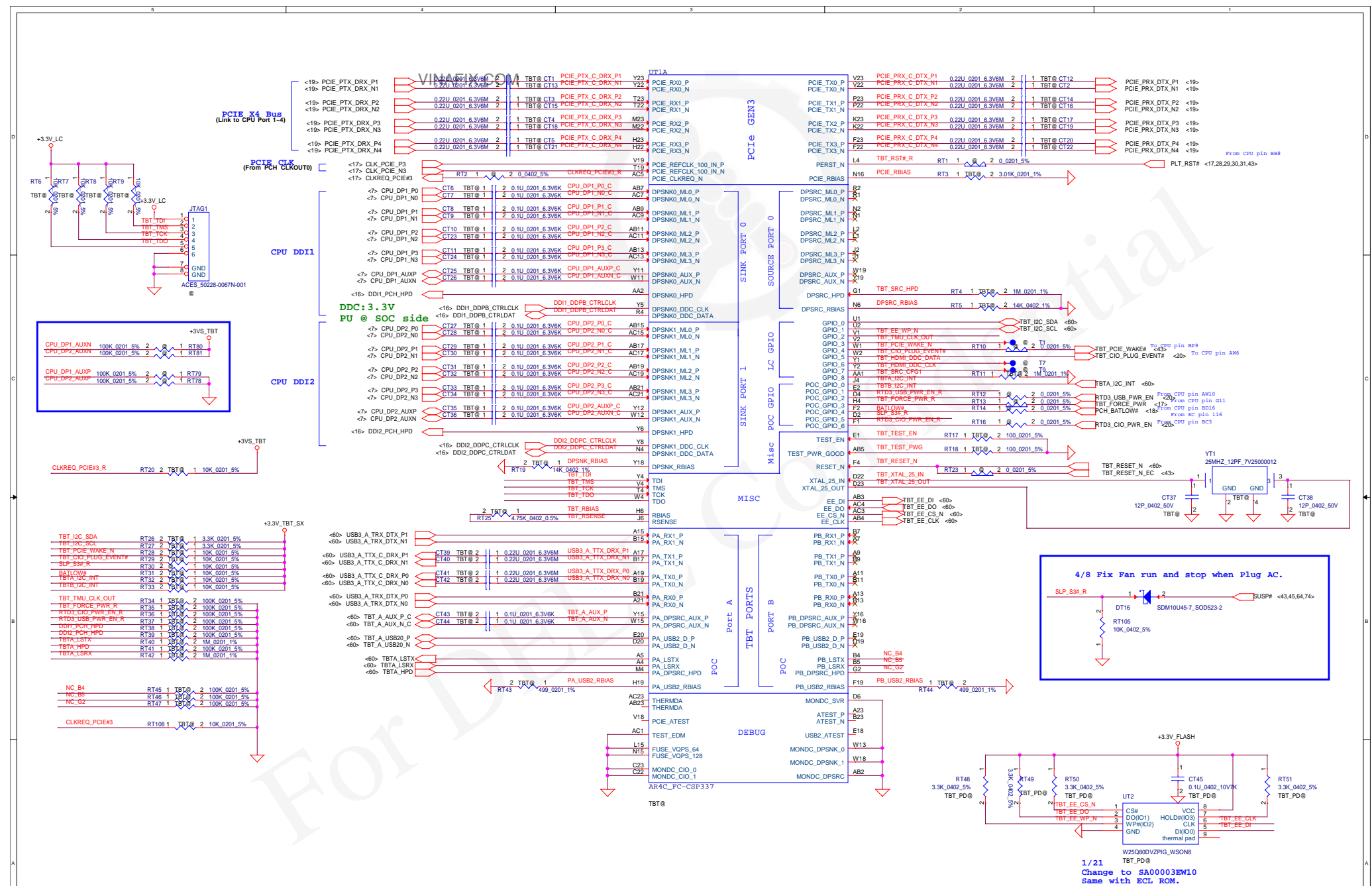
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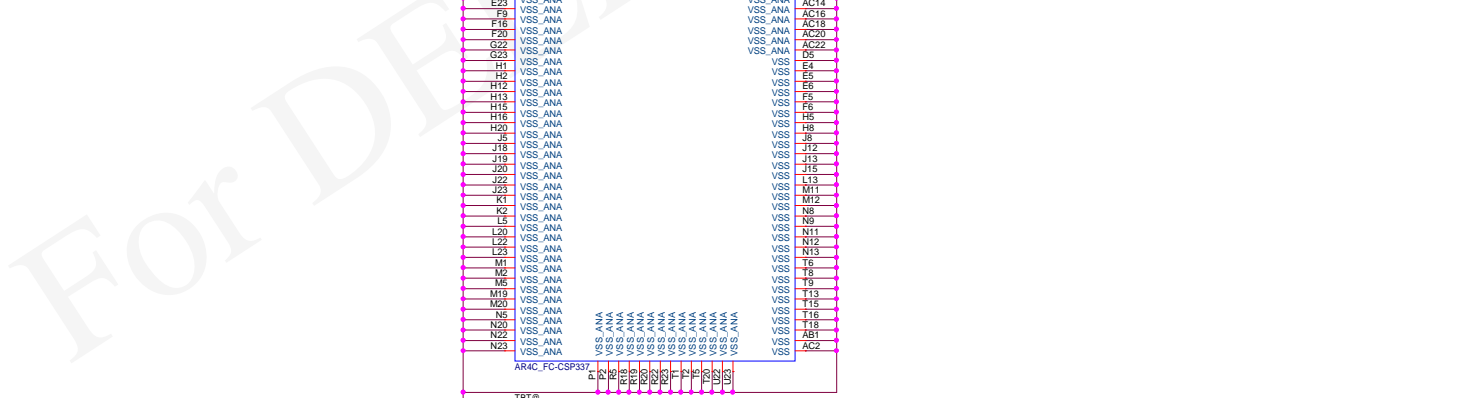
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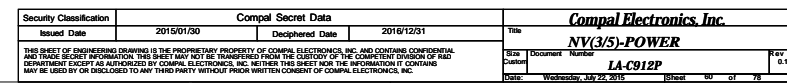
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				Size	Document Number
				Custom	LA-C912P
				Date	Wednesday, July 22, 2015
				Sheet	67 of 78
				Rev	0.1

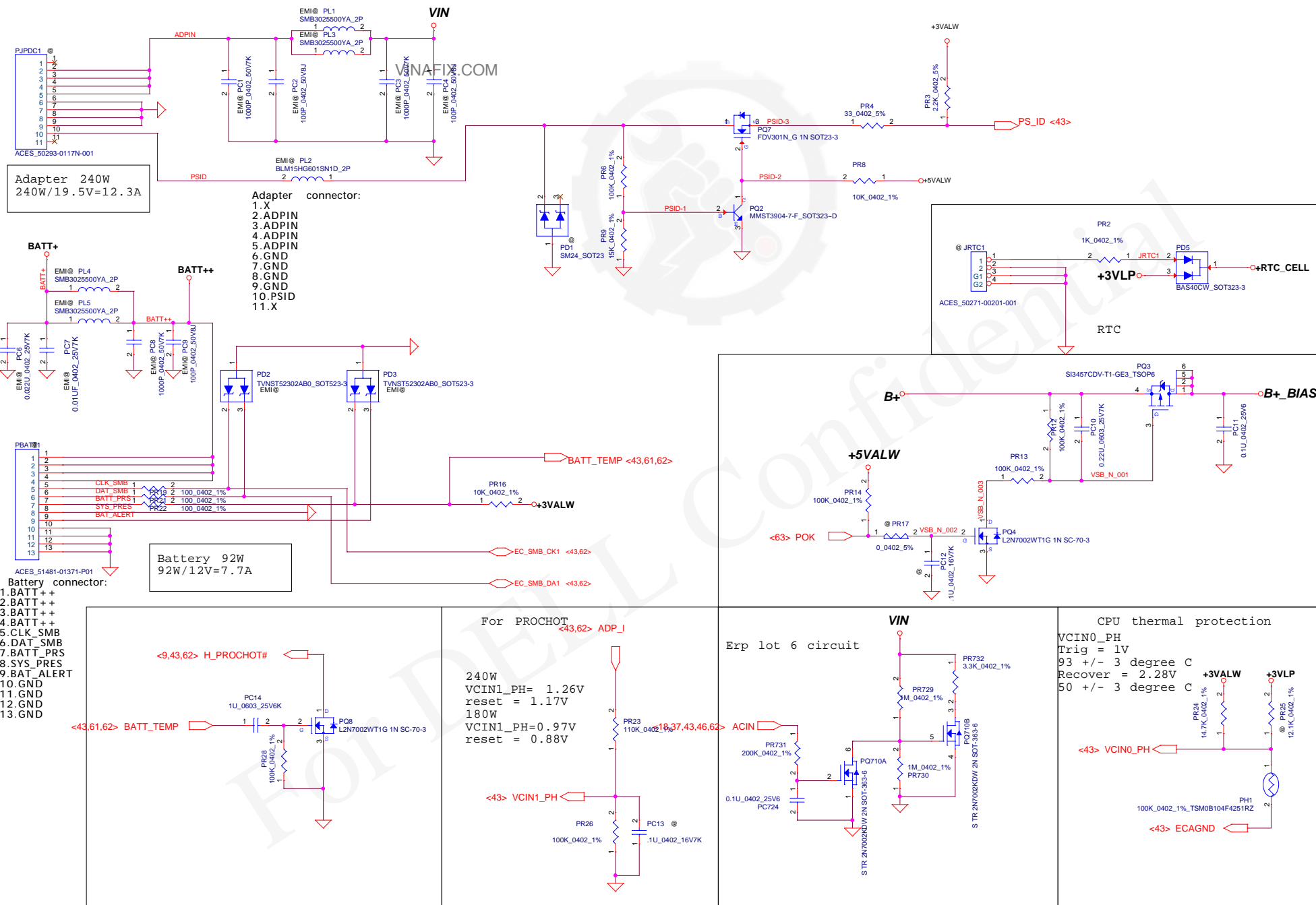


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				Custom	LA-C912P
				Date	Wednesday, July 22, 2015
				Sheet	58 of 78

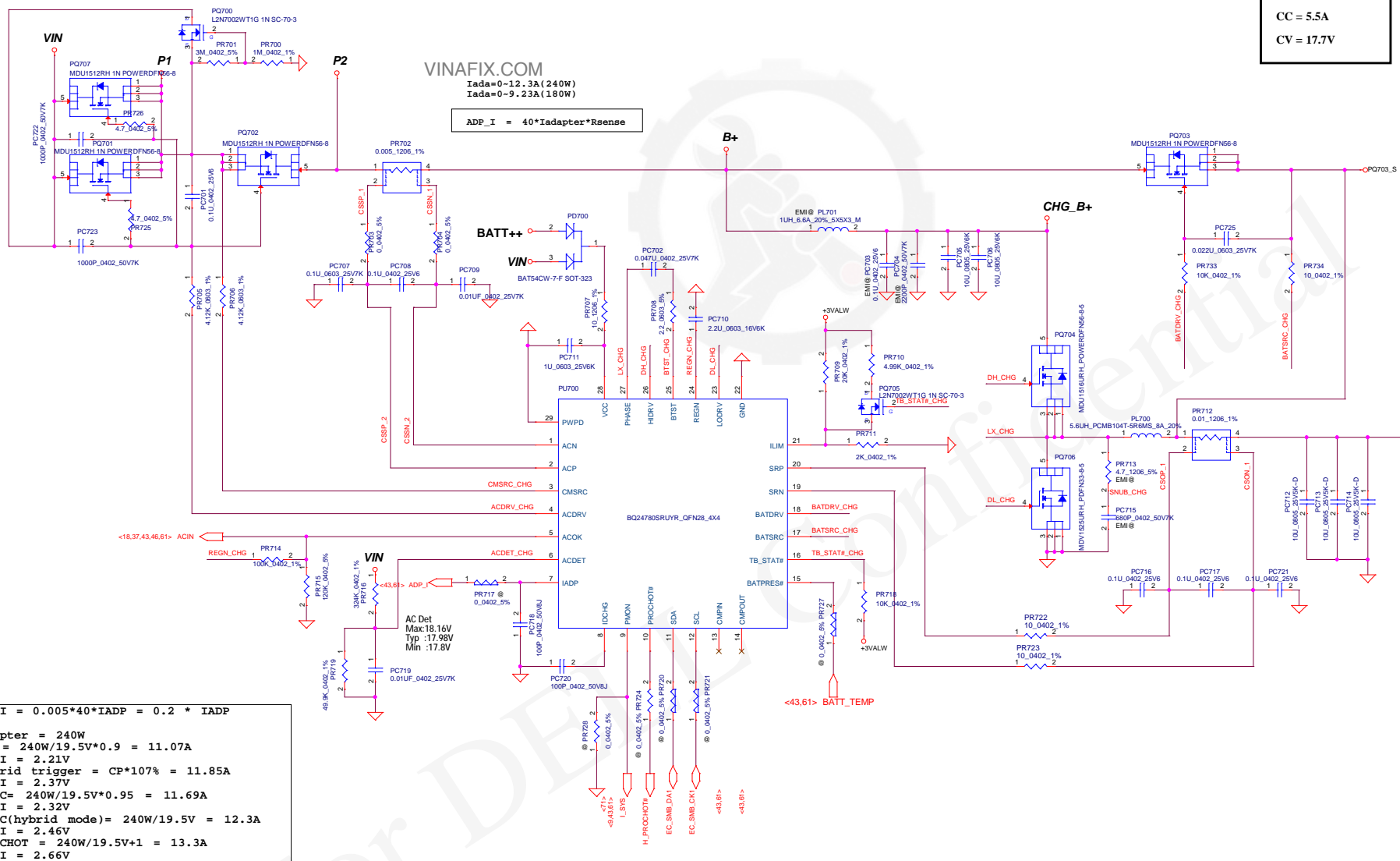


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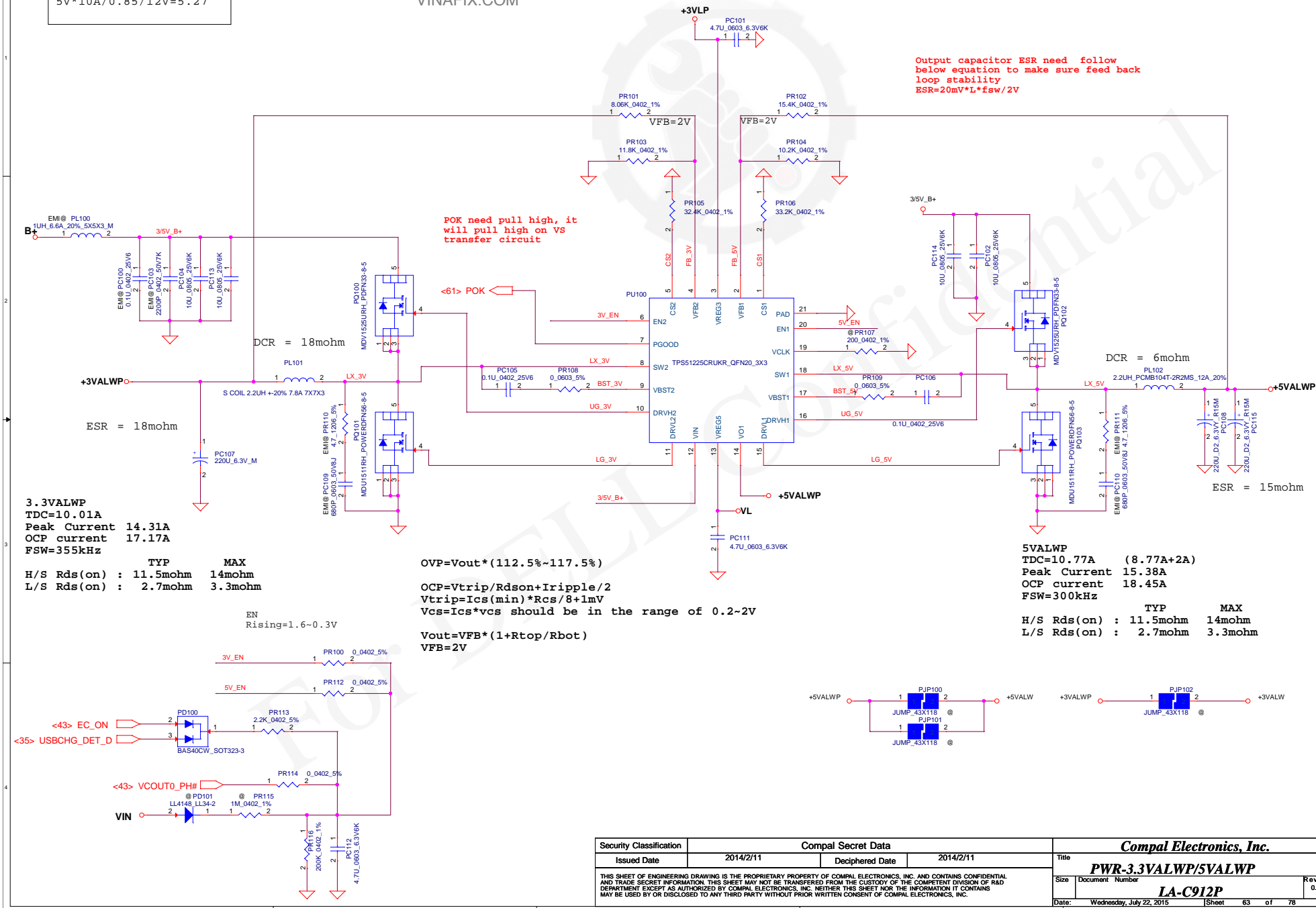
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Size		Document Number	LA-C912P	Rev 0.1
Date		Wednesday, July 22, 2015	Sheet	61 of 78



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Date: Wednesday, July 22, 2015				Rev 0.1
Sheet 02 of 78				LA-C912P

Input Current: 7.5A  
 $3.3V \times 10A / 0.85 / 12V = 2.23$   
 $5V \times 10A / 0.85 / 12V = 5.27$

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				Document Number
				LA-C912P
				Rev 0.1
				Date: Wednesday, July 22, 2015
				Sheet 63 of 78

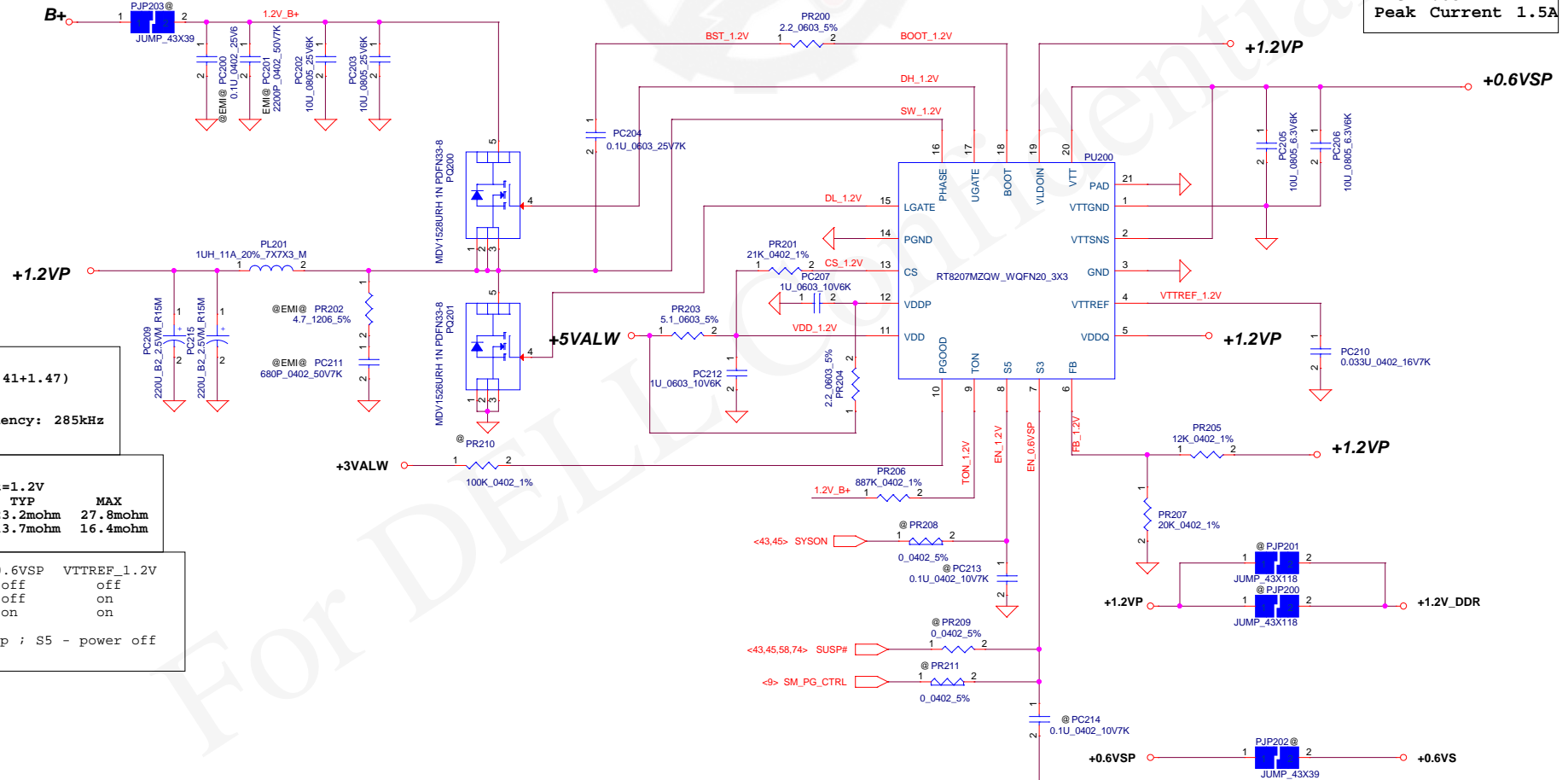


Input Current: 1A  
 $1.2V \times 8.88A / 0.85 / 12V = 1$

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Pin19 need pull separate from +1.2VP.  
 If you have +1.2V and +0.6V sequence question,  
 you can change from +1.2VP to +1.2VS.

0.6VSP  
 TDC 1.05A  
 Peak Current 1.5A



1.2VP  
 TDC=8.88A (7.41+1.47)  
 Ipeak=12.68A  
 OCP=15.21A  
 Switching Frequency: 285kHz

OVP: 110%~120%  
 VFB=0.75V, Vout=1.2V  

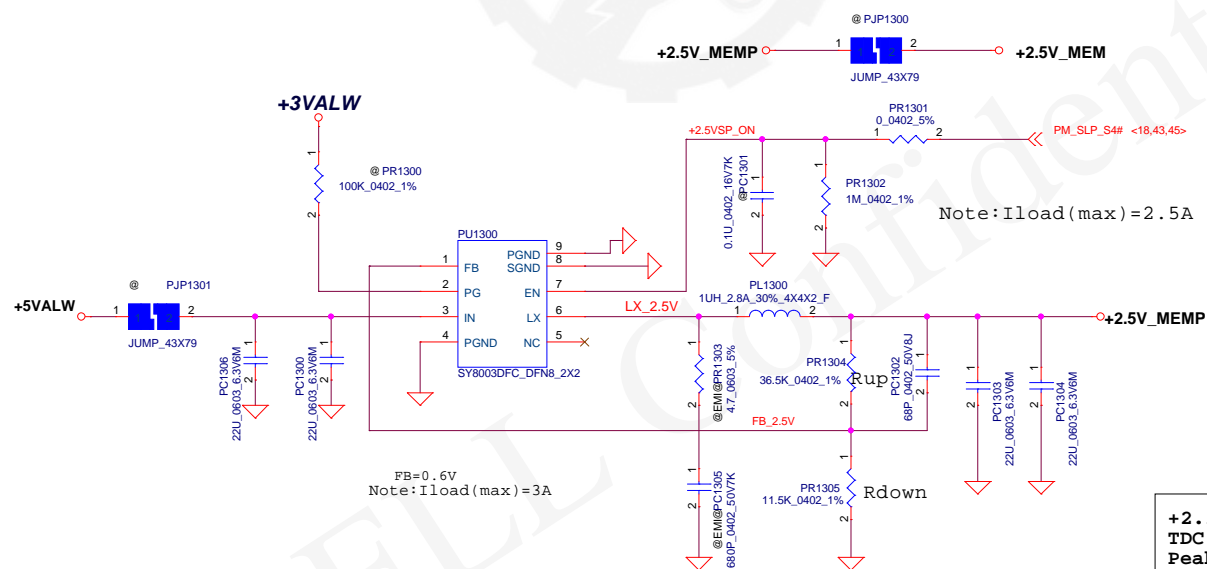
	TYP	MAX
H/S Rds(on)	23.2mohm	27.8mohm
L/S Rds(on)	13.7mohm	16.4mohm

Mode	Level	+0.6VSP	VTTREF_1.2V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

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Size	Document	Number	LA-C912P	Rev 0.1
Date:	Wednesday, July 22, 2015	Sheet	64	of 78

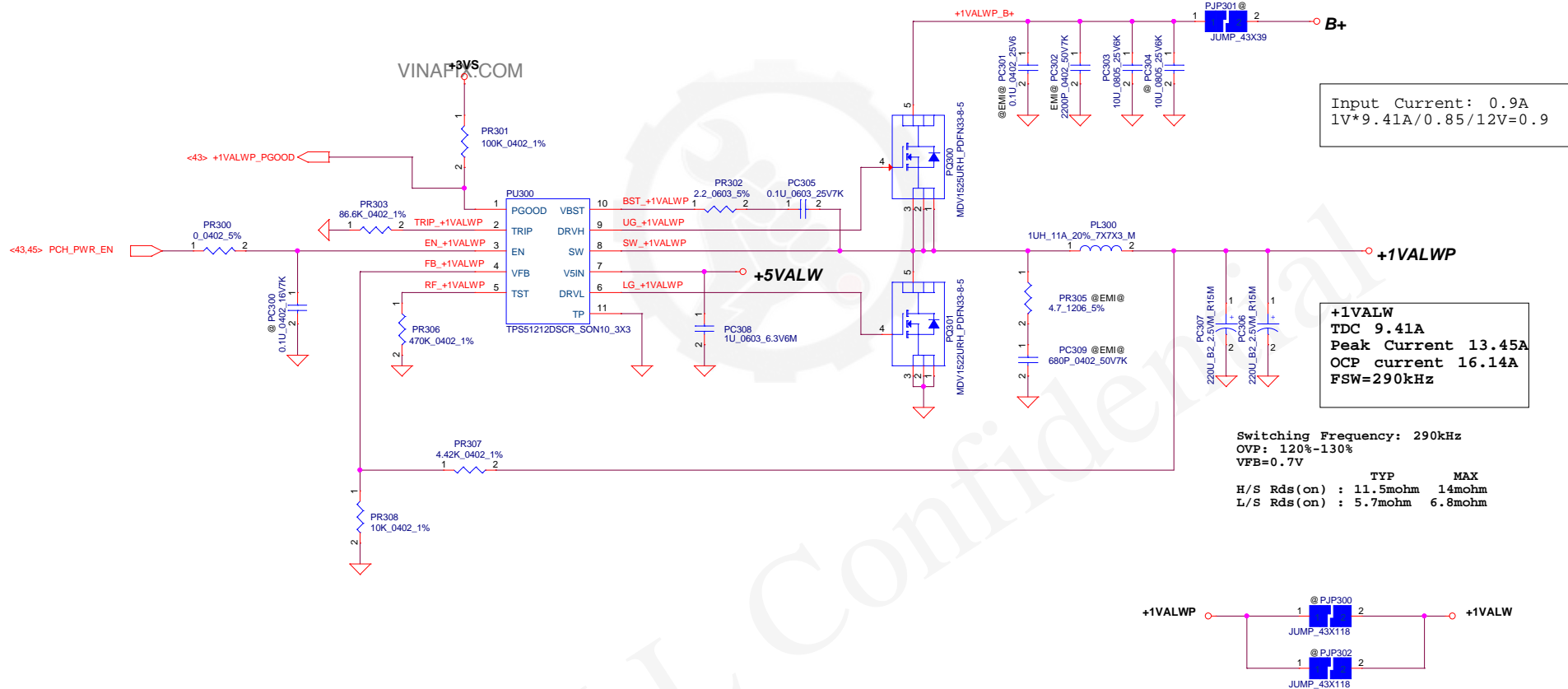




Note:  
When design  $V_{in}=5V$ , please stuff snubber  
to prevent  $V_{in}$  damage

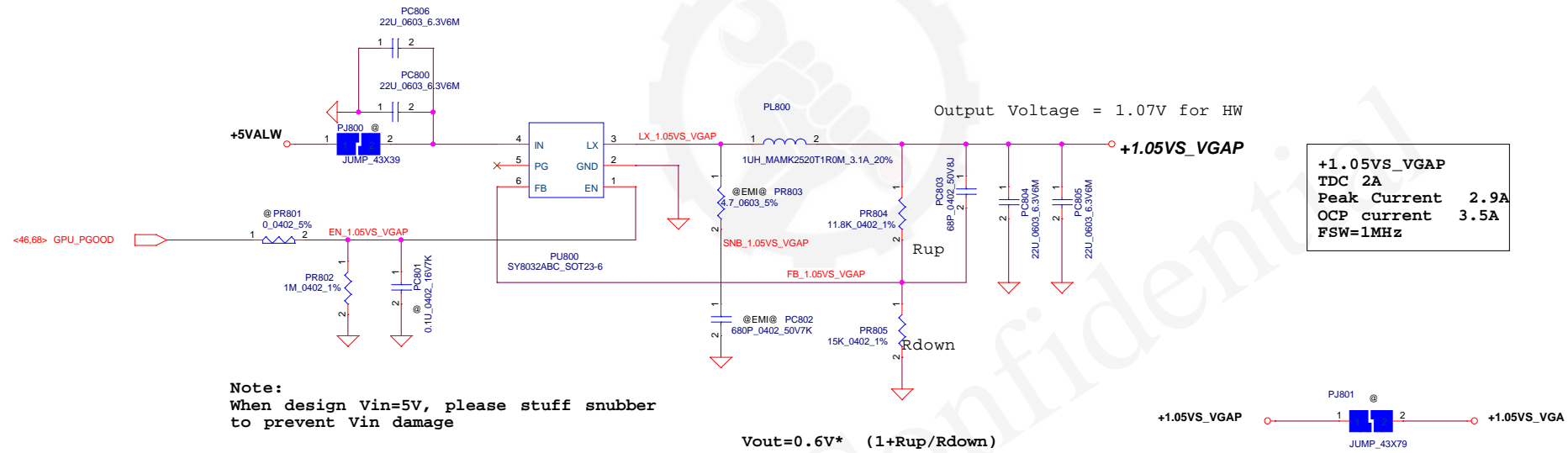
$$V_{out} = 0.6V * (1 + R_{up}/R_{down})$$

Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b>		
Issued Date	2014/2/11	Deciphered Date	2014/2/11	<b>PWR +2.5V MEM</b> <b>LA-C912P</b>		
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				Date:	Wednesday, July 22, 2015	Sheet 65 of 78

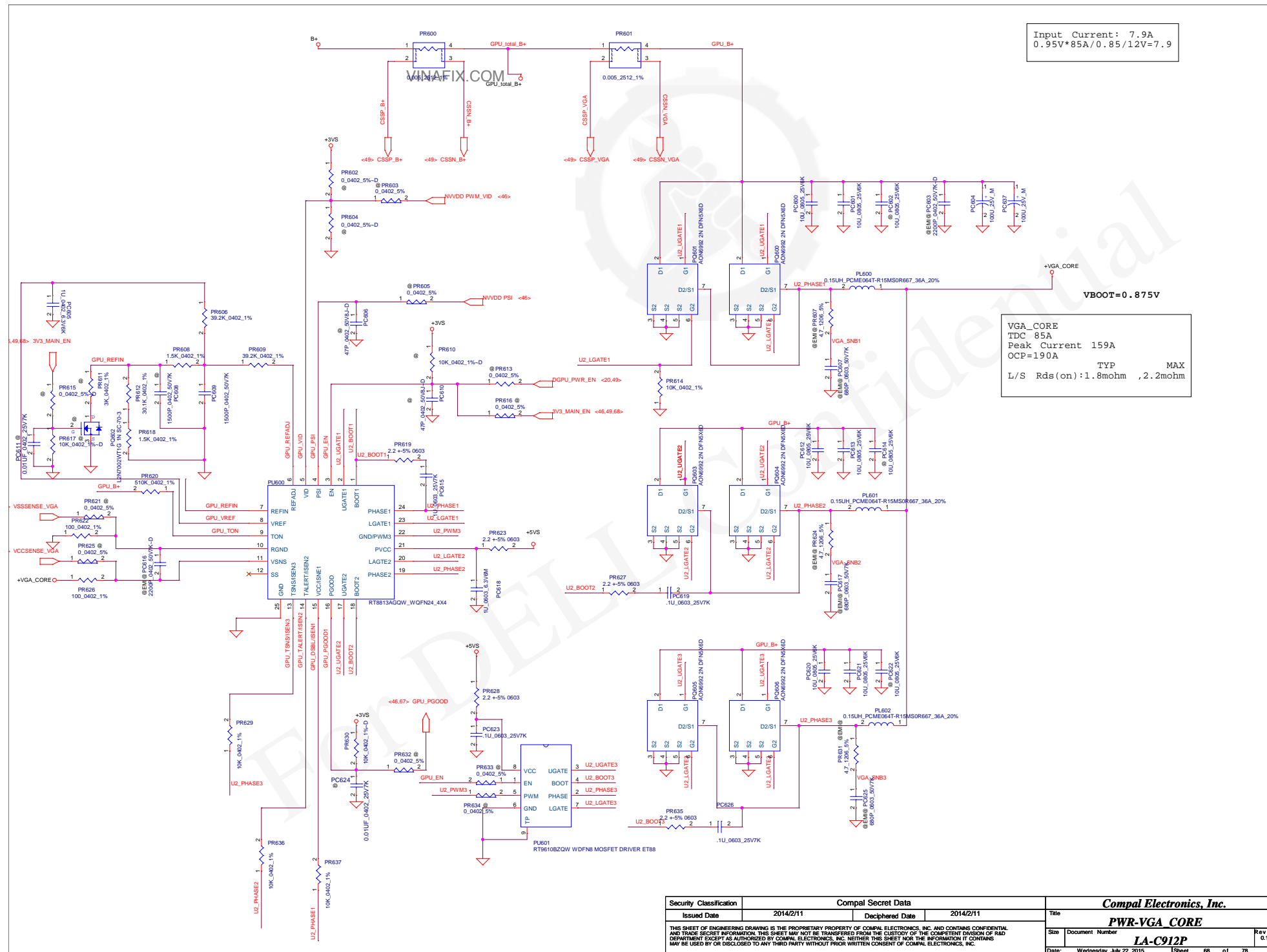


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					LA-C912P	0.1
				Date	Wednesday, July 22, 2015	Sheet 66 of 78

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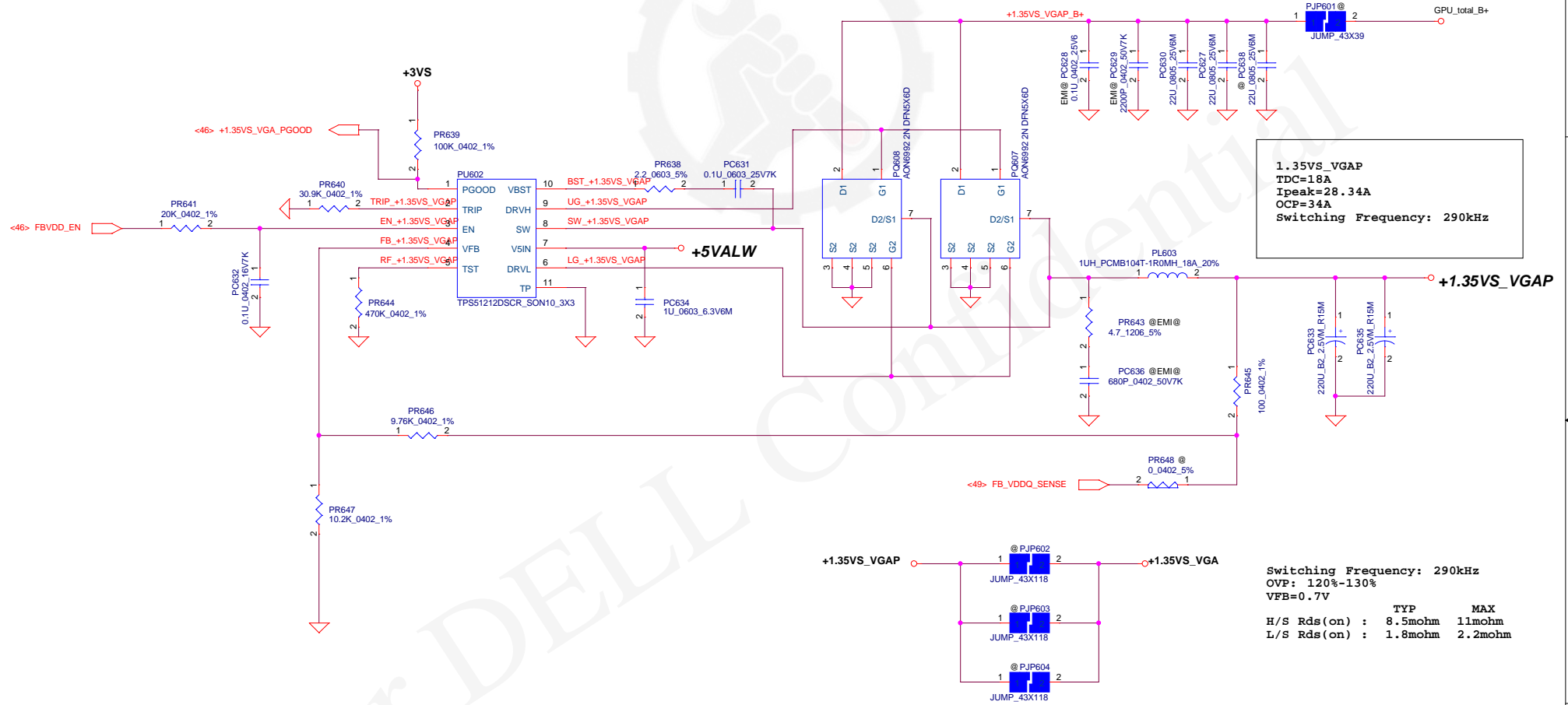


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Issued Date	2014/2/11	Deciphered Date	2014/2/11	Title		
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				Size	Document Number	Rev
				LA-C912P		
				Date	Wednesday, July 22, 2015	Sheet 67 of 78

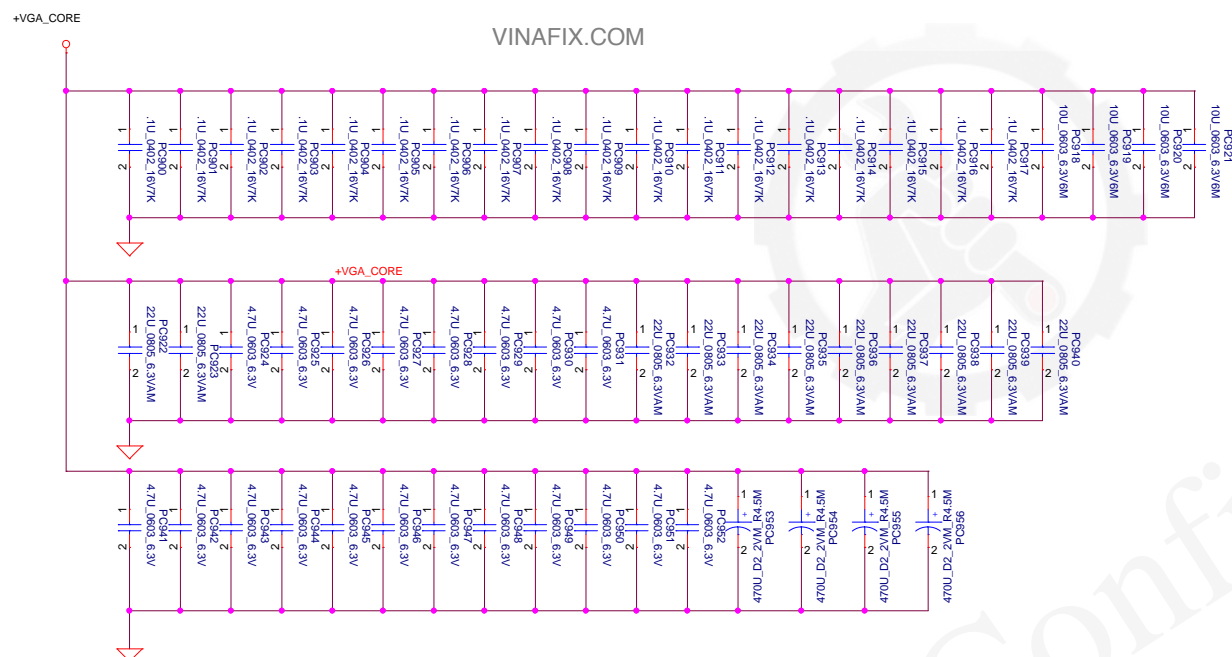


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Input Current: 2.4A  
 $1.35V \times 18A / 0.85 / 12V = 2.4$

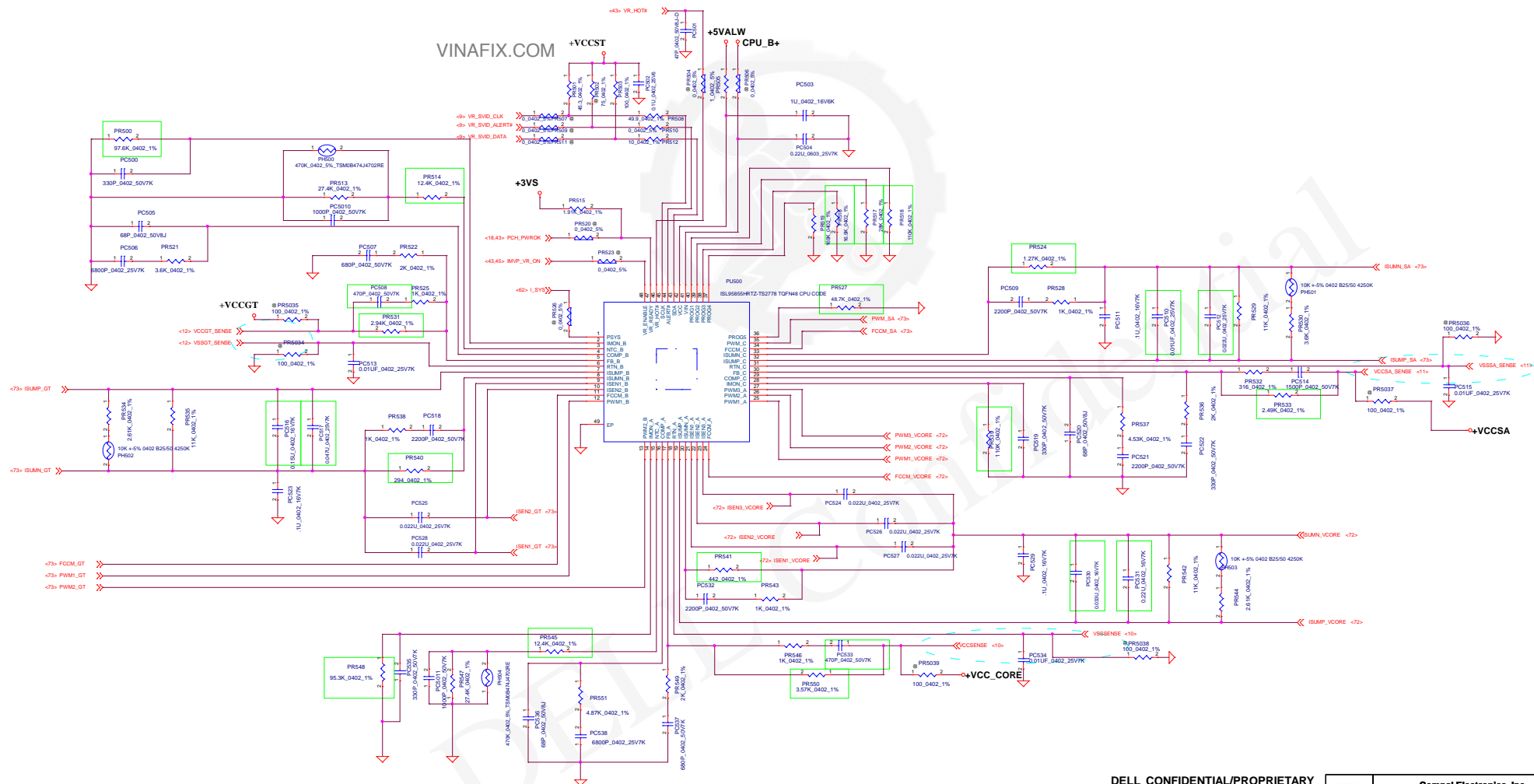


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Size		Document Number		Rev		0.1
Date:		Wednesday, July 22, 2015		Sheet		69 of 78



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				Size	Document Number	Rev. 0.
				<b>LA-C912P</b>		
Date: Wednesday, July 22, 2015				Sheet	70 of 78	

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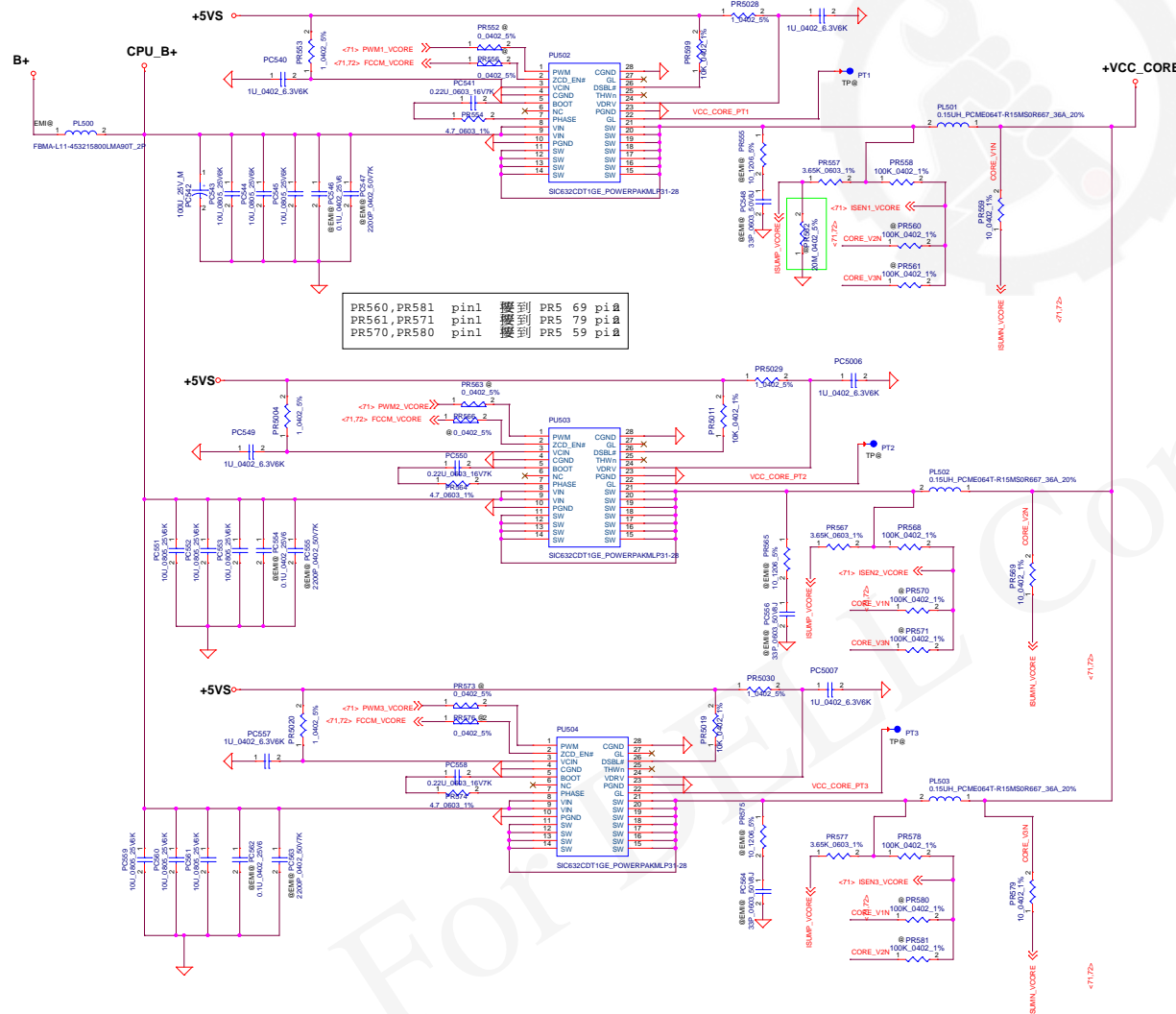


Compaq Electronics, Inc.	
PWR_VCORE_ISL95855	
Rev	0.1
Doc Number	LA-C912P
Date	Wednesday, July 23, 2003
Page	7.1 of 7.8

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Input Current: 8.2A  
 $1.5V \times 56A / 0.85 / 12V = 8.2$

```
VCC_CORE
TDC_PL2 :56A
Peak Current 68A
OCP Current 81.6A
DCR 0.66mohm +/-7%
Load Line 1.8mV/A
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**Compal Electronics, Inc.**

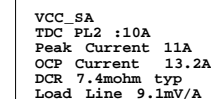
**PWR\_VCORE\_VCORE**

Number **LA-C912P**

	Re
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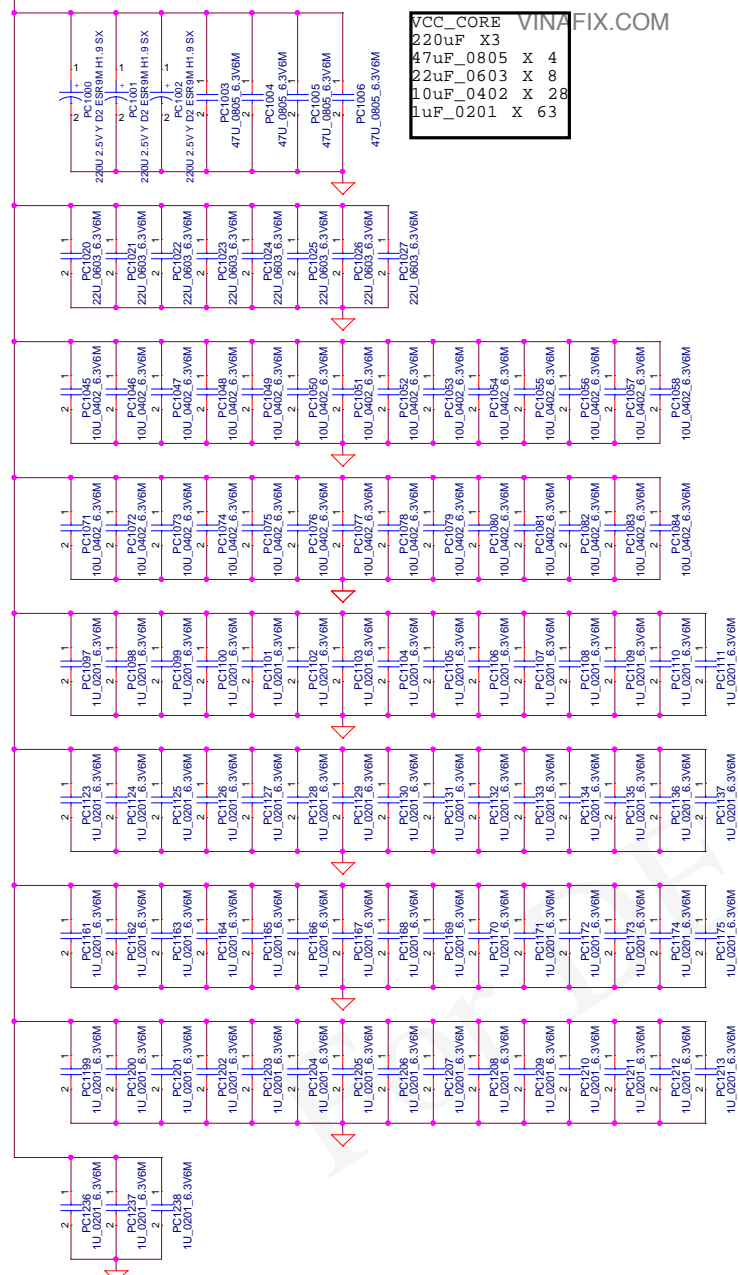




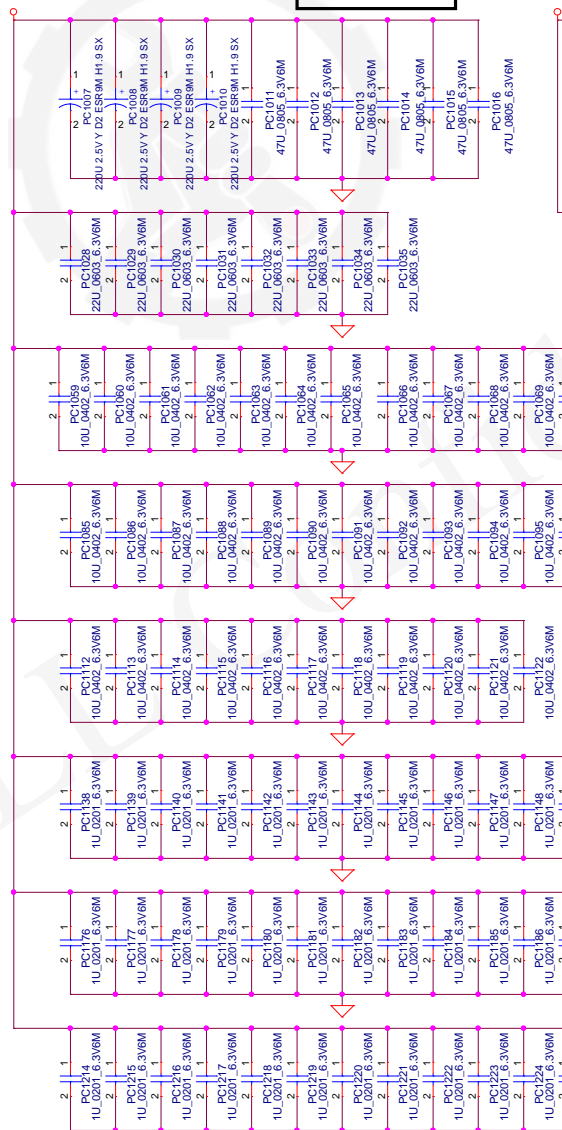
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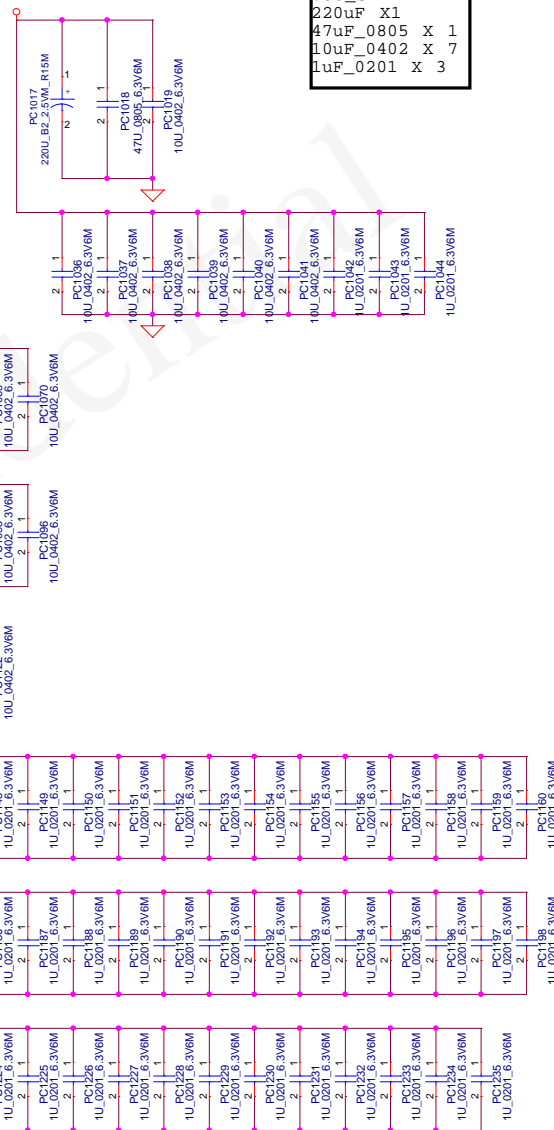
## +VCC\_CORE



## +VCCGT



## +VCCSA



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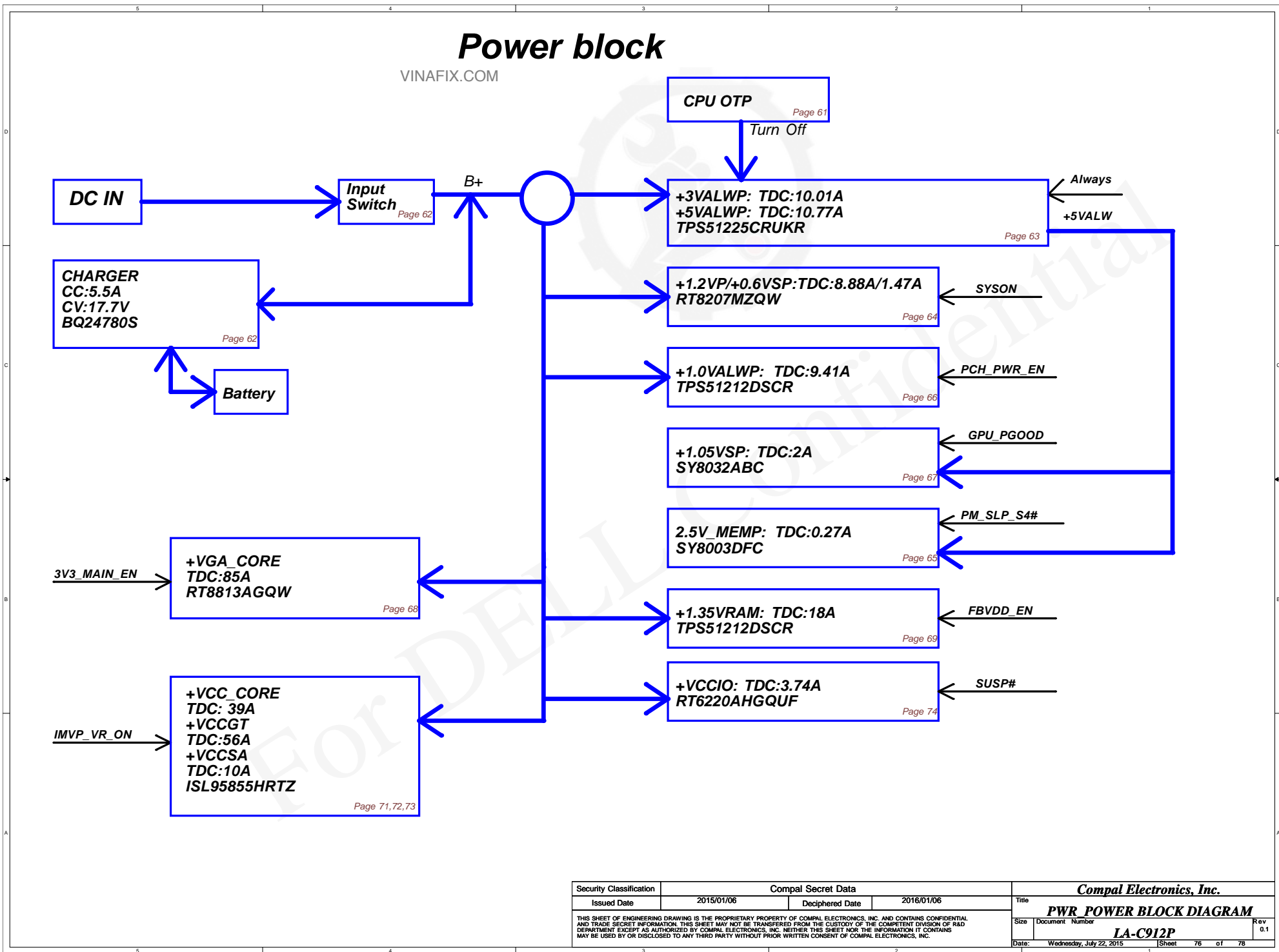


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LA-C911P

Date: Wednesday, July 22, 2015 Sheet 75 of 78



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					LA-C912P	0.1
				Date:	Wednesday, July 22, 2015	Sheet 76 of 78

## Version Change List ( P. I. R. List )

Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	68	PWR_+VGA_CORE	2015.4.1	Nick_Lin	Change VGA_CORE Choke	Change from S COIL .12UH 20% PCME063T-R12MS0R625 41A (SH00000QR00) to 0.15UH_PCME064T-R15MS0R667_36A_20% (SH00000U300) Location:PL600,PL601,PL602	
2	71	PWR_VCORE_ISL95855	2015.4.1	Nick_Lin	Change net from +1.0V_VCCST to +VCCST		
3	71	PWR_VCORE_ISL95855	2015.4.1	Nick_Lin	umount PR5034,PR5035,PR5036,PR5037,PR5038,PR5039	Change from 100_0402_1% (SD034100080) to @ Location:PR5034,PR5035,PR5036,PR5037,PR5038,PR5039	
4	66	PWR_+1VALWP	2015.4.11	Nick_Lin	Change OCP setting	Change from 210K_0402_1%_0402_1% (SD034210380) to 86.6K_0402_1% (SD034866280) Location:PR303	
5	69	PWR_+1.35VRAM	2015.4.11	Nick_Lin	Mount PC627 for Acoustic	Change from 10U_0805_25V (SE00000QK00) to 22U_0805_25V (SE00000XH80) Location:PC638	
6	69	PWR_+1.35VRAM	2015.4.11	Nick_Lin	Change PC630 for Acoustic	Add 22U_0805_25V (SE00000XH80) Location:PC627,PC630	
7	62	PWR_CHARGER	2015.4.11	Nick_Lin	Change PR702 for PMON function	Change from 0.004_1206_1% (SD000017Q00) to 0.005_1206_1%(SD000017R00) Location:PR303	
8	71	PWR_VCORE_ISL95855	2015.4.27	Nick_Lin	Change ISL95855 circuit by FAE advice	Change form SD000009480 (S RES 1/16W 1.47K +-1% 0402) to SD034127180 (S RES 1/16W 1.27K +-1% 0402) Location PR524 Change form SD000009M80 (S RES 1/16W 2.61K +-1% 0402) to SD00000UV00 (S RES 1/16W 3.6K +-1% 0402) Location PR530 Change form SE068221J80 (S CER CAP 220P 25V J NPO 0402) to SE074152K80 (S CER CAP 1500P 50V K X7R 0402) Location PC514 Change form SD034100180 (S RES 1/16W 1K +-1% 0402) to SD000003480 (S RES 1/16W 316 +-1% 0402) Location PR532 Change form SE074681K80 (S CER CAP 680P 50V K X7R 0402) to SE074331K80 (S CER CAP 330P 50V K X7R 0402) Location PC522 Change form SD034100180 (S RES 1/16W 1K +-1% 0402) to SD034453180 (S RES 1/16W 4.53K +-1% 0402) Location PR537 Change form SD034113380 (S RES 1/16W 113K +-1% 0402) to SD034110380 (S RES 1/16W 110K +-1% 0402) Location PR539 Change form SE075223K80 (S CER CAP 0.022U 25V K X7R 0402) to SE076333K80 (S CER CAP .033U 16V K X7R 0402) Location PC530 Change form SD034267080 (S RES 1/16W 267 +-1% 0402) to SD034301080 (S RES 1/16W 301 +-1% 0402) Location PR541 Change form SE074222K80 (S CER CAP 2200P 50V K X7R 0402) to SE074471K80 (S CER CAP 470P 50V K X7R 0402) Location PC533	

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					LA-B751P	0.1
				Date:	Wednesday, July 22, 2015	Sheet 77 of 78

## Version Change List ( P. I. R. List )

Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
9	71	PWR_VCORE_ISL95855	2015.4.27	Nick_Lin	Change ISL95855 circuit by FAE advice	Change form 'SD034100180 (S RES 1/16W 1K +-1% 0402) to 'SD034487100 (S RES 1/16W 4.87K +-1% 0402) Location PR511 Change form 'SE075223K80 (S CER CAP 0.022U 25V K X7R 0402) to 'SE00000MJ00 (S CER CAP 0.047U 25V K X7R 0402) Location PC517 Change form 'SE074222K80 (S CER CAP 2200P 50V K X7R 0402) to 'SE074471K80 (S CER CAP 470P 50V K X7R 0402) Location PC508 Change form 'SD034182180 (S RES 1/16W 1.82K +-1% 0402) to 'SD00000UV00 (S RES 1/16W 3.6K +-1% 0402) Location PR521 Change form 'SD034953280 (S RES 1/16W 95.3K +-1% 0402) to 'SD034976280 (S RES 1/16W 97.6K +-1% 0402) Location PR500	
10	71	PWR_VCORE_ISL95855	2015.6.24	Nick_Lin	Change VCC_CORE VR_IMAX	Change form 'SD034301080 (S RES 1/16W 301 +-1% 0402) to 'SD034442080 (S RES 1/16W 442 +-1% 0402) Location PR541 Change form 'SD034243180 (S RES 1/16W 2.43K +-1% 0402) to 'SD034357180 (S RES 1/16W 3.57K +-1% 0402) Location PR550 Change form 'SD034562180 (S RES 1/16W 5.62K +-1% 0402) to 'SD034280280 (S RES 1/16W 28K +-1% 0402) Location PR517 Change form 'SD034931280 (S RES 1/16W 93.1K +-1% 0402) to 'SD034953280 (S RES 1/16W 95.3K +-1% 0402) Location PR548	
11	71	PWR_VCORE_ISL95855	2015.6.24	Nick_Lin	Change VR_ProcHOT Trig point	Change form 'SD034105280 (S RES 1/16W 10.5K +-1% 0402) to 'SD00000AJ80 (S RES 1/16W 12.4K +-1% 0402) Location PR545,PR514	
12	61	PWR_DCIN / BATT CONN / OTP	2015.6.24	Nick_Lin	fine tune OTP setting	Change form 'SD034162280 (S RES 1/16W 16.2K +-1% 0402) to 'SD034147280 (S RES 1/16W 14.7K +-1% 0402) Location PR24	

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					LA-B751P
				Date:	Wednesday, July 22, 2015
				Sheet	78 of 78
				Rev	0.1